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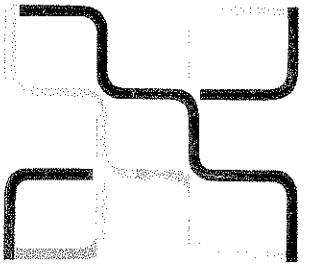
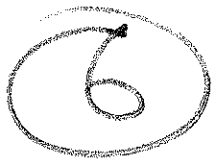
PROTEUS COMPUTER

Technical manual

Issue 1. 8/12/82





PROTEUS COMPUTER

Technical manual

Issue 1. 8/12/82

PROTEUS COMPUTER
Technical Manual

1. GENERAL

The PROTEUS computer is a unique 64Kbyte computer with both Z80 and 6809 micro-processors. Two 8" disk drives are included which give a total on-line storage of over 1Mbyte. There is an RS232 port for connection to a terminal and printer, and also an ADLC port for connection to a network of POLY-1 computers.

The computer can run the following operating systems-

1. CP/M. The standard operating system for 8080/Z80 micros.
2. FLEX. The standard operating system for 6809 micros.
3. POLYSYS. The operating system for the POLY network.

1.1 Dual Processors.

Either the Z80 or the 6809 can be running at a given time, but not both. The two processors can however pass control to each other. The system always starts with the 6809 running and the Z80 remains reset. The 6809 reads in the first sector on the disk and starts execution of it. If it is a FLEX or POLY disk the the system operates exactly as before. If it is a CP/M disk one of the first few instuctions halts the 6809 and starts up the Z80. The rest of CP/M is then loaded and executed.

1.2 Ports.

Only one RS232 port is available. This is connected to a terminal with a controlled printer port eg ADM-21. When the CP/M I/O software (BIOS) detects output to the printer it automatically sends control charaters to the terminal to select the 'transparent print' mode - and the following output is sent to the printer without being displayed on the screen. The normal mode is reselected in a similar manner when output to the screen resumes. BIOS may easily be modified to use the control codes applicable for various terminals.
Although ADM-31 and ADM-42 terminals do work in the above manner they do not handshake correctly when printing.
The terminal must be set for conversational mode,full duplex,9600 baud, 8 data bits, no parity, 1 stop bit. The printer interface on the terminal must be set to suit the printer. If an EPSON printer is used with an ADM-42 a special cable must be used which connects pin 20 of the printer to pin 19 of the ADM-42.

1.2.1 RS232 Port

Baud Rate : 300,600,1200,2400,4800,9600 Selectable by jumper.
Protocol : 8 data bits, no parity, 1 stop bit.
Connector : DB25 Female connector on PROTEUS.

- Pin 1 : GROUND
- Pin 2 : TXDATA Data transmitted by terminal to PROTEUS.
- Pin 3 : RXDATA Data transmitted by PROTEUS to terminal.
- Pin 5 : CLEAR TO SEND Normally high level output by PROTEUS. Can be set low by software.
- Pin 6 : DATA SET READY High level output by PROTEUS.
- Pin 7 : GROUND
- Pin 8 : DATA CARRIER DETECT High level output by PROTEUS.
- Pin 20 : DATA TERMINAL READY High level output by terminal when it is ready to receive data. No data will be transmitted by PROTEUS while this line is low.

1.2.2 Network Port.

5 pin NEUTRICK microphone connector. Male connector on PROTEUS.

- Pin 1 : Data out from PROTEUS.
- Pin 2 : Clock out from PROTEUS.
- Pin 3 : Ground.
- Pin 4 : Data in to PROTEUS

1.3 Disks.

The normal CP/M format used is single density, double sided. 512 byte physical sectors are used with code to block and deblock the 128 byte logical sectors of CP/M. Single sided with 128 byte sectors can be used for transfer to other CP/M systems. A utility must be used to select single sided operation on a given drive. It is considered that the double sided blocked format will always be used, except for interchange with other CP/M systems.
With FLEX and POLYSYS single or double sided need only be defined at the time of formatting the disk. 256 byte sectors are used.

1.3.1 Disk capacity.

	FLEX-POLYSYS	CP/M
Sides	2	2
Tracks/side	77	77
Sectors/track	15	8
Bytes/sector	256	512
Total formatted capacity/disk	591360	630784

In both systems the sectors on side 2 are numbered as a continuation of the sectors on the same track on side 1.

1.4 Polycorp Utilities

Utility programs have been written to format disks, check newly formatted or used disks for CRC errors, select single sided etc.

The Polycorp utilities are in the file UTE1.COM which displays a menu of the available commands. As yet there is no fast disk to disk copy program or a single drive copy program. The command file PUTSYS should be used to copy the operating system onto a disk.

The standard CP/M utilities all operate as described in the CP/M manual execpt that it is not possible to change the physical to logical device assignments with the STAT command, and PUTSYS should be used rather than SYSGEN.

1.5 CP/M Software

In addition to the operating system itself the following software has been used with complete success on the CP/M system-

MBASIC	Microsoft Basic ver 5 for CP/M
MACRO-80	Microsoft 8080 / Z80 Macro Assembler
LINK	Linking loader
ZSID	Z80 symbolic debugger
WORDMASTER	Screen editor
WORDSTAR	Word processor

Notes:
1. Wordmaster and Macro-80 are infinitely better than ED and ASM, the editor and assembler supplied with CP/M. Wordstar is even better used in its non-document mode for writing program code.
2. If an ADM-21 terminal is used with Wordstar be sure that it has the 4k Z8 fitted. With the initial 2k it was far too slow. When installing Wordstar select ADM-31 for ADM-21, ADM-31, ADM-42 and Televideo 910+.

1.6 Low-level CP/M programming notes

Interupts are not normally used in the CP/M system. If they are required the Z80 must be programmed for Interupt Mode 1. A jump instruction to the interupt service routine must then be inserted at address 0038H. Note that this restart is the same as that normally used by the debugger ZSID for breakpoints and tracing - however ZSID can be patched to use another restart.

If it is required to use the timer chip in the Z80 mode it should be noted that the E input which is 1MHz in the 6809 mode will not be a constant frequency. However a fixed 1MHz signal has been connected to the external clock inputs of the timer and it should be programmed to use that.

1.7 Memory maps

In the Z80 mode the I/O ports are shifted to the Z80 I/O space and the EPROM is deselected. This gives 64k of RAM.

FLEX memory map

Address	Type	Contents
0000 BFFF	RAM	User RAM (Large transient progs)
C000 DFFF	RAM	FLEX operating system (Small transient programs)
E004-5 E014 E018-B E020-7 E030-6 E060	I/O	ACIA - 6850 Drive register FDC - 1771 PTM - 6840 ADLC - 6854 Enable Z80
F000 FFFF	ROM	BOOTSTRAP,6809 DEBUGGER ETC

CPM memory map

Address	Type	contents
0000 00FF	RAM	CPM Variables etc
0100 DFFF	RAM	TPA (Transient Program Area)
E000 E7FF	RAM	CCP (Console command processor)
E800 F5FF	RAM	BDOS (Basic Disk Operating System)
F600 FFFF	RAM	BIOS (Basic Input-Output System

CPM I/O MAP

04-05	ACIA - 6850
14	Drive register
18-1B	FDC - 1771
20-27	PTM - 6840
30-36	ADLC - 6854
50	Enable 6809

2.0 Z80-6809 Processor PCB

2.1 General Description

U7,U8 are the two microprocessors. Their address and data busses are connected in parallel, and it is arranged so that when each one is operating the other is in a high impedance state.

U10,U11,U33 are used to generate timing signals from the Z80 which more or less correspond to those generated by the 6809.

U25,U26 select the control and I/O decode signals from the 6809 or the Z80, depending on which is running.

U27 decodes the memory addresses in the E000-EFFF range in the 6809 mode and decodes the I/O port addresses in the Z80 mode. It should be noted that the decoded signals are disabled during the first part of any machine cycle (when the address lines are all changing) so that glitches do not occur on the outputs.

U28 is the disk bootstrap and debug ROM. It is accessible only in the 6809 mode.

U30 is used to keep time of day and to generate the clock signal for the network only when running POLYSYS.

U30 is the data link control IC.

U12-U19 are the 64k x 1 dynamic memories.

U22 is the refresh counter. As an 8 bit refresh address is generated, memory ICs which require 7 or 8 bit refresh addresses can be used.

U20,U21 select the refresh address instead of the CPU address during the refresh operations.

U23,U24 are the row/column address multiplexor used to multiplex the 16 bit CPU address onto the 8 address pins of the memory ICs.

2.2 Operation of Dual Processors

The simplified operation of the dual processor is as follows-
The control signals required for the memory and I/O are generated by the 6809 more or less directly. The Z80 control signals are manipulated so that they approximate those generated by the 6809. A data selector is then used to select the source of the control signals for the rest of the system depending on which processor is running.

2.3 Clock Oscillator

A 4MHz oscillator (U4,X1,Q1) is used to drive the clock inputs of both the 6809 and Z80. This results in the 6809 operating at a (bus) frequency of 1MHz. One wait state is inserted into each machine cycle of the Z80 to reduce its bus frequency to approximately 1MHz also.

2.4 Generation of control signals

With the 6809 in control RAS is activated when Q goes high. The address lines of the memory chips are switched when E goes high. CAS is activated when Q goes low. Finally when E goes low the cycle is complete and RAS and CAS are de-activated. Refresh of the memory occurs during cycles when E000 or above is addressed ie I/O, ROM or internal operations. RAS is generated as above but CAS is not generated. Instead of the CPU address being selected the refresh counter is selected during the entire refresh cycle and incremented at the end of the cycle.

With the Z80 in control RAS is activated on the first positive clock edge after MREQ is activated. This is also the start of the wait state. The address lines are switched on the next negative edge of the clock. CAS is then activated on the next positive edge of the clock. At the end of MREQ, RAS and CAS are both de-activated. Refresh occurs during the RFSH output of the Z80 which is used to select the refresh counter and to increment it. RAS is generated by U11a during the refresh operation.
The control signals are generated in a similar manner during I/O cycles. RAS is also generated on the first positive clock edge after IOREQ is asserted. (This refreshes a random memory address!) On the folowing negative clock edge "E" is generated as required by the 6800 family peripherals. "E" is also generated during memory cycles as it is the same signal as the multipexor control.

2.5 Transfer of control

When the PCB is reset the 6809 is always selected. To transfer control to the Z80, the 6809 should execute a double byte store instruction to $E060. This will halt the 6809 at the end of the instruction and at the same time remove the reset from the Z80. After a couple of clock cycles the Z80 will start execution of the instruction at 0000. This instruction must have been put there by the 6809.

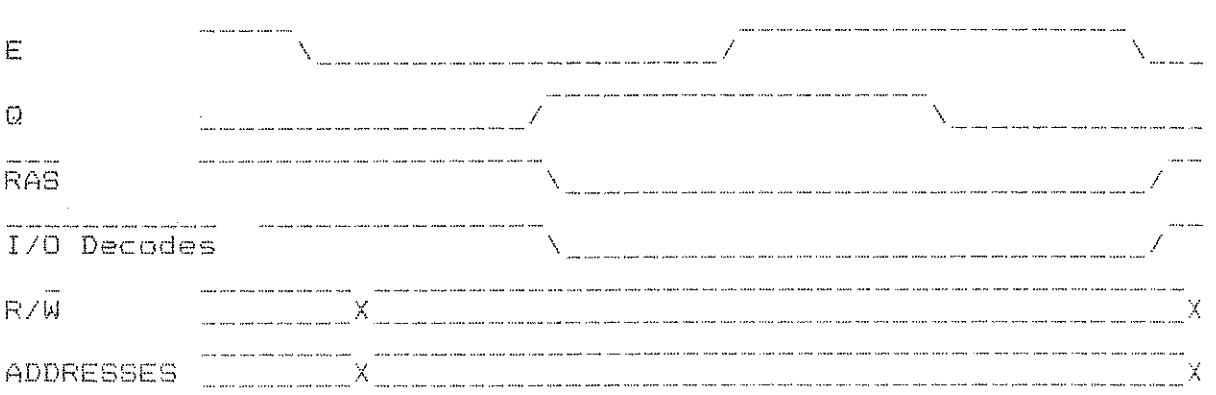
To transfer control back to the 6809, the Z80 should execute an output to I/O port 50. This will immediately reset the Z80 and the 6809 will continue operation with the instruction following the double byte store insruction which it used to halt itself.

It should be noted that when the switch is made from one set of control signals to the other, by altering the state of the select input to U25,U26, that all of the control signals are always inactive.

2.6 6809 Timing Diagram

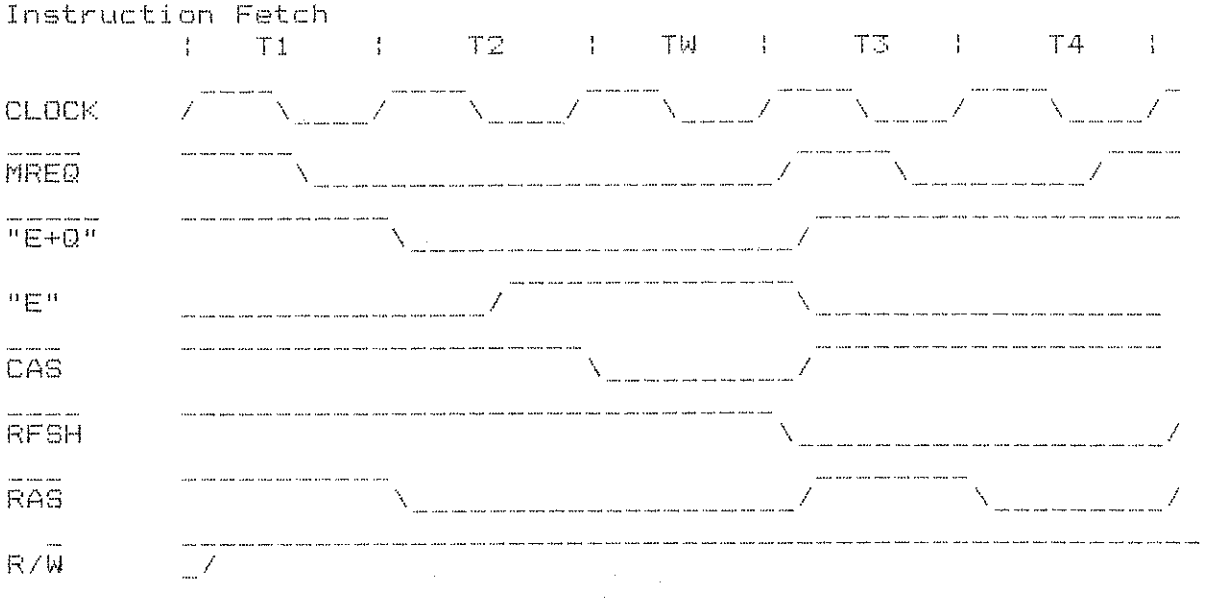
Memory cycle

I/O cycle

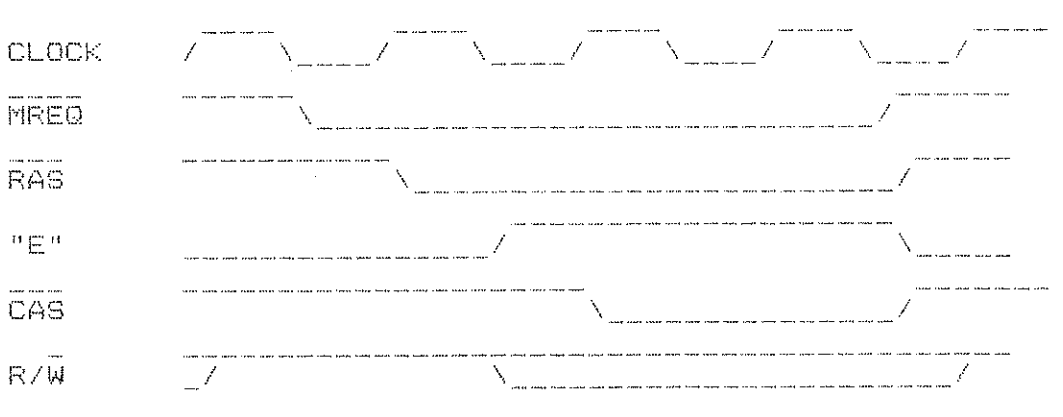


2.7 Z80 Timing Diagram

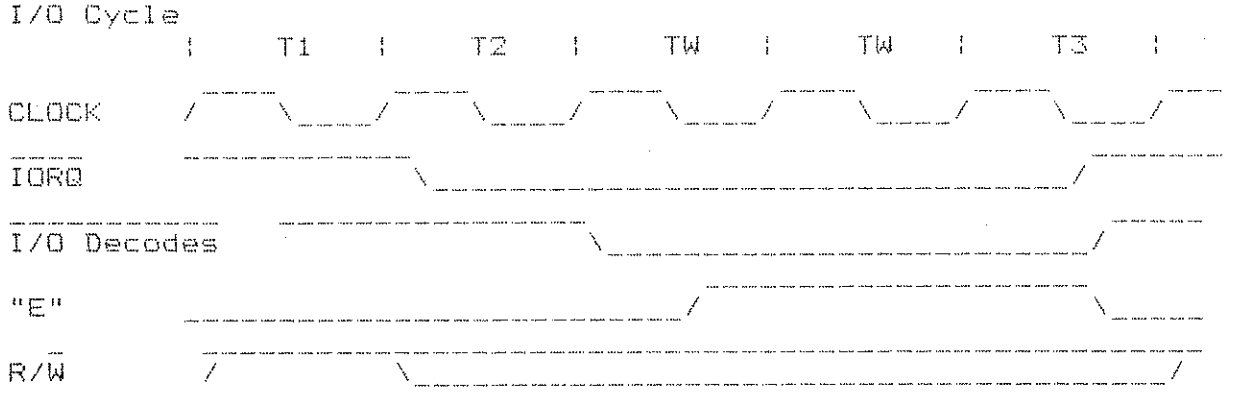
Instruction Fetch



Memory Reference



I/O Cycle



3.0 Disk Controller PCB

3.1 General

U12 is the floppy disk controller IC which performs most of the fuctions required for the floppy disk interface.

U15 is the inverting data bus buffer used to connect the logic true bus of the CPU to the logically inverting data bus of the floppy disk controller IC.
U7 is the drive and side select register.

U16 is used to enable the drive select signals for 3 seconds after any CPU access to the disk controller.

U1,U3,U4 are the driver ICs for the disk drive interface.

U5 is the receiver IC for the disk drive interface.

U13,U17,U9,U10 are the data separator circuit.

U19 is the ACIA ie interface for the serial RS232 interface.

U6,U11 are the driver and receiver ICs for the RS232 interface.

U14,U18 are the baud rate generator for U19.

3.2 Drive and side select

Address E014 (I/O port 14) is the write-only drive select register. The lower 2 bits define the drive-

00 = drive 0 or A
01 = drive 1 or B

Other codes are invalid as there are only two drives.
Bit 6 is the side-select control-

0 = side 1 (or 0!)
1 = side 2 (or 1!)

The drive selects are enabled for approximately 3 seconds after the last disk access. After the disk has not been accessed for this time, all drives will be deselected and the red indicaters will be extinguished. The TANDON drives normally fitted will stay turning for 30 seconds after this time after which their motors are stopped.

3.3 Disk Change Detector

The Disk-change output from the selected drive can be read by the CPU reading location E014 bit 1. If it is a 1, the disk drive door has been opened since the drive was last selected. This bit is cleared when the drive is deselected.

3.4 Floppy disk controller

The FD1771 IC performs all the reading, writing, and head stepping functions required by the floppy disk system. For more information the manufacturers data sheet should be consulted.

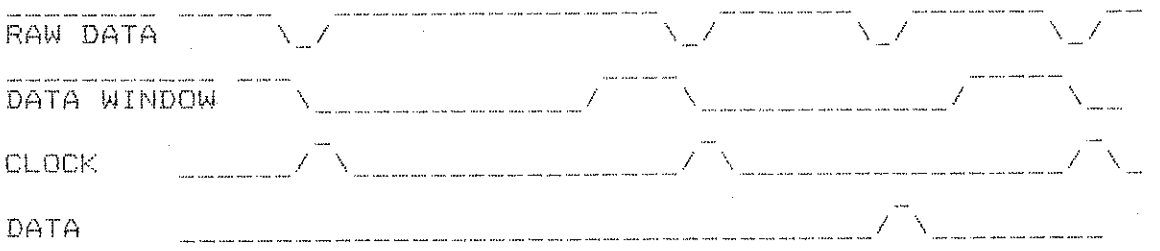
3.5 Data Separater

The output from the drive consists of clock pulses (nearly) every bit boundary (every 4 microseconds), and data pulses midway between the clock pulses if the data bit is a 1. If the data bit is a 0 there is no data pulse.
The data separater basically consists of a 3 microsecond monostable triggered by the clock pulses. If another pulse arrives during this time it is considered to be a data pulse. The data and clock pulses are routed to separate inputs of the 1771.
This simple operation is complicated by the fact that during address marks and other special marks on the formatted disk there are missing clock pulses used to identify the special marks. When this happens U13a, which is triggered by data pulses, is used to trigger U13b at around the time that it would normally be triggered by a clock pulse. At the end of 3 consequeutive missing clock pulses, U21 pin 6 goes low which resets the monostable and determines that the next pulse will be taken as a clock pulse. This normally happens during the special marks and also if the separater starts off with the data and clock pulses around the wrong way.
U10c and U10d are used to ensure that a change in the data window generated by U13b cannot take effect during a data or clock pulse.

3.6 Data separater alignment

1. Load the head on a formatted disk.
2. Monitor U10 pin 12 with an oscilloscope and adjust RV1 until the length of the negative going pulses is 3.0 microseconds.
3. Monitor U17 pin 11 with the oscilloscope and adjust RV2 until the bright negative going pulse PLUS the dim extension is 2.7 microseconds.

3.7 Data separater timing diagrams



4.0 Power Supply

The power supply is a conventional transformer/ capacitor input filter/ linear regulator design. The transformer has 3 windings-

1. 27.3 Vac (used for 24v dc)
2. 9.4 Vac (used for 5v dc)
3. 14.1 Vac (used for +12v,-12v,-5v dc)

The regulator assembly produces the following supplies for EACH drive-
+24v +- 10% at 1.5 A intermittent
+5v +- 5% at 0.7 A

and the following supplies for the computer and interface PCBs
+12v +- 10% at 50mA
+5v +- 5% at 0.7 A
-5v +- 10% at 1mA
-12v +- 10% at 50mA

The power supply is capable of maintaining the above outputs with a mains voltage of 200-260 volts.

5.0 Production Testing

The CPU board and disk interface board are tested with the EXORCISOR plugged into the 6809 socket using the program MINI64. This tests most of the board except for the Z80 associated components.
If the boards pass the above test it should be able to boot FLEX. The Z80 circuitry can then be tested with the program Z80-6809. The memory should then be tested with the program MTEST64. The disk drives should then be checked by copying the complete contents of a disk onto the other drive and back again using the FLEX MIRROR command. Finally it should be verified that CP/M will run by booting a CP/M disk.

				Each	Total
1	Chassis	To dwg	1		
2	Cover	To dwg	1		
3	Disk drive	Tandon 848/2 / Shugart 860	1 or 2		
4	Fan.	Rotron Sprite SU3A1	1		
5	Transformer	McKenzie & Holland 110WU163	1		
6	Mains switch	DJ Reid SW28	1		
7	Reset switch	DJ Reid SW16	1		
8	Neon indicator	DJ Reid N6YL	1		
9	Washer for neon	" " N6	1		
10	Clip for neon	" " N4	1		
11	Mains filter	Sprague 2JX5102A OR Schaffner FN610-3/06	1		
	Fuse holder	DJ Reid FH1	1		
13	Fuse	" " FSBL1	1		
14	Terminal strip.	PDL 2way	1		
15	Insulated Faston terminals	AMP 735278	42		
16	* Disk DC Power connector TANDON housing	AMP 1-480270-0	1 or 2		
17	* Pins for above (female) TANDON	AMP 163300-6	3 or 6		
18	Rectifier	MDA 3501	2		
19	Connector to disk interface bd.	Blue Mars 609-5030 / Robinson Nugent IDS-50PK	1		
20	Connector to drive PCB	Blue Mars 609-5015M / Robinson Nugent IDE-50	1 or 2		
21	Ribbon cable 50 way	Blue Mars 171-50 / RIN CAB-50	0.6m		
	RS232 connector panel mtg	Cannon CEA-134-DB25S OR DJ Reid CS25S	1		
23	Stainless steel lugs	Utilux 1964	5		
25	Jumper for Disk Change.	Molex M7859-Gold	1		
26					
27	Mains plug	PDL 40	1		
28	Mains cable	0.75 mm² Abcal TPS white	3m		
29	Cable anchor	DJ Reid HW121 type A	1		
30					
31	Alt. to Item 16 for shugart drive Disk DC Power Connector	AMP 1-480763-0	2		
32	Alt. to Item 17 for shugart drive Pins	AMP 350550-1	6		
33					
34					

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Date		

Parts List for Universal Twin Disk

				Each	Total
1	Rubber feet	Philips 3123 104 0353	4		
2	PCB mtg extrusion	To drwg (LEDA plastics)	1.5m		
3	Network connector	Ventrick NC5FP	1		
4	Reset switch connector housing	M6671-2A	1		
5	Network cable housing	M6471-6A	1		
6	RS232 cable housing	M6671-8A	1		
7	DC Power cable housing	M3011-5B	1		
8	0.1" terminal	M2759-GL	17		
9	0.2" terminal	M2578-GL	5		
10	Hookup wire 0.5mm²	DJ Reid WIA9 xx	10m		
11	0.6mm².	" WJL03 xx	10m		
12					
13	Power Supply PCB assembly	see list "Twin disk Power Supply PCB"	1		
14	Z80/6809 PCB assembly	see list "Z80 6809 PCB assy"	1		
15	Disk controller PCB	see list "Disk Controller PCB assy"	1		
16	Bus PCB	see list "Bus PCB"	1		
17					
18	Serial number sticker	NZ Labels	1		
19	Rear panel label	McKenzie & Holland 'Poly Disk Unit'	1		
20	Front panel badge		1		
21					
22	Cable ties.	130 mm cable ties.	20		
23	Screws for drive	AN-503-832-6	8		
25					
26	Miscellaneous screws.				
27					
28					
29					
30					
31					
32					
33					
34					

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Parts List for
Universal Twin Disk Unit

				Each	Total
1	V1, V2.	L200CV	2		
2	V3, V4, V5	7805	3		
3	V6	7812	1		
4	V7	7912	1		
5	D1, D2	1N4004	2		
6	D3	BZY79/B5V1	1		
7					
8	C1	6800μF40v. ROE	1		
9	C2	10000μF25v ROE	1		
10	C5, C6	1000μF25v 2222-034-66102	2		
11					
12	C3, C4, C7-C16	1μF50v TANT. STC.	12		
13					
14	R2, R4	6K2 1% 2322-151-56202	2		
15	R1, R3	820 1% 2322-151-58201	2		
16	R5	1KSFR25 2322-181-53102	1		
17					
18	Heatsink	(Included in chassis dwg.)	1		
19	PCB	820806	1		
20					
21	Faston lugs.	Zettrich Z836	18		
22					
23					
25					
26					
27					
28					
29					
30					
31					
32					
33					
34					

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Parts List for
Twin Disk Unit
Power Supply PCB Assy.

Sheet 1 of 1

				Each	Total
1	U1	SN 74LS08	1		
2	U2, U6	SN 74LS00	2		
3	U3	SN 74LS02	1		
4	U4, U9	SN 74LS 04	2		
5	U5	SN 74LS 10	1		
6	U7	Z80A -CPU	1		
7	U8	MC 6809	1		
8	U10	SN 74LS175	1		
9	U11	SN 74LS74	1		
10	U12-U19	all 200 nsec. MCM 6665 / TMS 4164 / MSK 4164	8		
11	U20, U21, U23, U24, U25, U26	SN 74LS157	6		
12	U22	SN 74LS 393	1		
13	U27	SN 74LS 138	1		
14	U28	TMS 2532	1		
15	U29	MC 6840	1		
16	U30	MC 6854	1		
17	U31	1488	1		
18	U32	1489	1		
19	U33	SN 74LS 73	1		
20	(U31-U32) skts	16 pin DIL skt. RIN ICN-163-S3-TG	2		
21	(U12-U19) skts	16 pin DIL skt RIN ICN-163-S3-TG	8		
22	(U28) skt	24 pin DIL skt RIN ICN-246-S4-TG	1		
23	(U29, U30) skt	28 pin DIL skt RIN ICN-286-S4-TG	2		
25	(U7, U8) skt	40 pin. Samtec IC-640-SGT	2		
26	R1, R2	1K SFR25 2322-181-53102	2		
27	R3	1K2 SFR25 2322-181-53122	1		
28	R4	220 SFR25 2322-181-53221	1		
29	R5	27 SFR25 2322-181-53279	1		
30	R6, R10-R20	47 SFR25 2322-181-53479	12		
31	R7, R8, R9, R21	3K3 SFR25 2322-181-53332	4		
32					
33	Q1	BC557	1		
34					

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Parts List for
Z80/6809 PCB Assy

				Each	Total
1	X1	6MHz series HC18-U resonant crystal	1		
2					
3	C1	100pF 63v Murata RD870	1		
4	C2	39pF 63v " "	1		
5	C3	22MF 16v electro. 2222-034-65229	1		
6	C4, C5	56pF 63v Murata RD870	2		
7	C10 - C44	0.1MF 63v Seimens.	35		
8					
9	D1, D2	IN4148	2		
10					
11	Reset connector	M4030-2AG	1		
12	LED connector	M4030-3AG	1		
13	Network connector	M4030-4AG	1		
14					
15	Edge connector.	M4455-10AG	1		
16	" "	M4455-20AG	1		
17	Polarising Pin	M4161-1	1		
18	PCB	820706	1		
19					
20					
21					
22					
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25					
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28					
29					
30					
31					
32					
33					
34					

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Parts List for

Z80/6809 PCB Assy

				Each	Total
1	U12	FD1771 B-01	1		
2	U19	MC 6850	1		
3	U16	MC 14538	1		
4	U6	MC1488	1		
5	U11	MC1489	1		
6	U9, U10	SN 74LS00	2		
7	U8	SN 74LS04	1		
8	U2	SN 74LS08	1		
9	U5	SN 74LS14	1		
10	U1, U3, U4	SN7438 (9322 414 60112)	3		
11	U17, U21	SN 74LS74	2		
12	U20	SN 74LS138	1		
13	U7	SN 74LS175	1		
14	U18	SN 74LS191	1		
15	U13	SN 74LS221	1		
16	U14	SN 74LS393	1		
17	U15	SN 74LS640	1		
18	(U6, U11)	14 pin DIL skt ICN-143-S3-TG	2		
19	(U19)	24 pin DIL skt ICN-206-S4-TG	1		
20	(U12)	40 pin DIL skt ICN-406-S4-TG	1		
21	C2, C3	100pF 63v Murata RD870	2		
22	C1 + unreferenced decoupling	0.1μF 63v Seimens	14		
23	C4	1μF 30v Tantalum	1		
25	R1, R2, R3, R4, R5, R6	150Ω ¼FR25 2322-181-53151	6		
26	R13	470Ω " " " 53471	1		
27	R7	3K3 " " " 53332	1		
28	R11	22K " " " 53223	1		
29	R12	680K " " " 53684	1		
30	R10	3M3 MR25 2322-211-12335	1		
31	R9	27K MR25 2322 151 52703	1		
32	R8	33K " " " 53303	1		
33	RV1, RV2	20K Cermet Pot Spectrol 63S203	2		
34	C5	22p 63v Murata RD870	1		

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Date	4/5/82

Parts List for

Disk Controller PCB

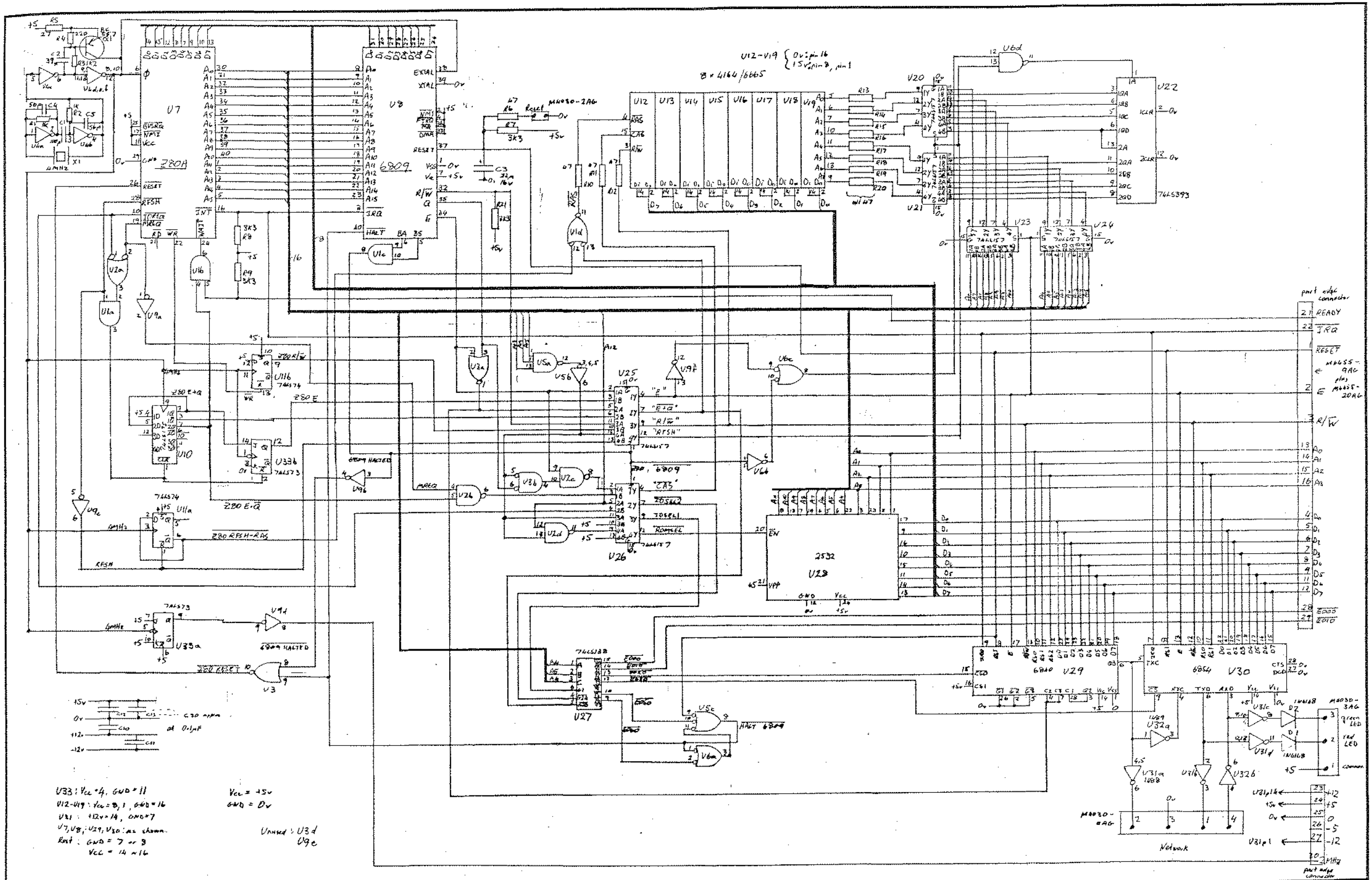
				Each	Total
1	RS232	8 pin wafer M 4030-8AG	1		
2	Band rate	14 pin wafer M 4030-14AG	1		
3	Edge con.	10 pin edge con. M4055-10AG	1		
4	" "	20 pin edge con. M4055-20AG	1		
5	PCB	PCB 820302	1		
6	Band rate selector	Jumper M7859 Gold	1		
7	Polarizing pin	M4161-1	1		
8	Connector to drive cable	Blue Mac, 609-5007	1		
9		OR GR R/N IDH-50PK-SR3	1		
10		+ EL-2K	2		
11					
12					
13					
14	RVS PCB				
15		9 pin wafer M4030-9AG	2		
16		20 pin wafer M4030-20AG	2		
17		5 pin wafer M3003-5AG	1		
18					
19		PCB 820304	1		
20					
21					
22					
23					
25					
26					
27					
28					
29					
30					
31					
32					
33					
34					

POLYCORP

Date 4/5/82

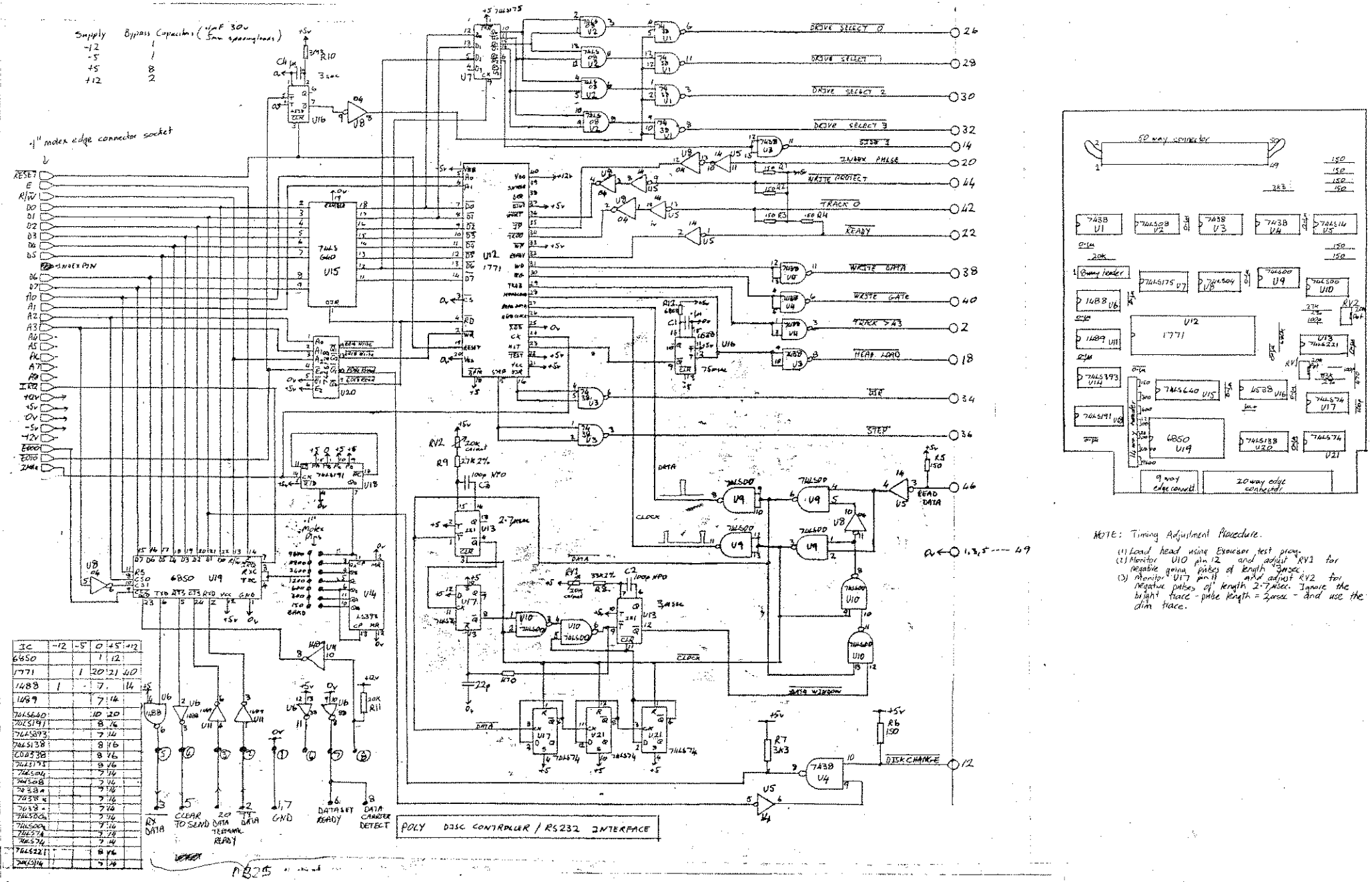
Parts List for

Disk Controller PCB



POLYCORP

Z80 /6809 PROCESSOR			SHEET
DRAWN	CHECKED	SCALES	SERIES OF
TRACED	DATE		REF



NOTE: Timing Adjustment Procedure.

(1) Load head using Exerciser test prog.
(2) Monitor U10 pin 12 and adjust RV1 for negative going pulses of length 3μsec.
(3) Monitor U17 pin 11 and adjust RV2 for negative pulses of length 2.7μsec. Ignore the bright trace - pulse length = 3μsec - and use the dim trace.

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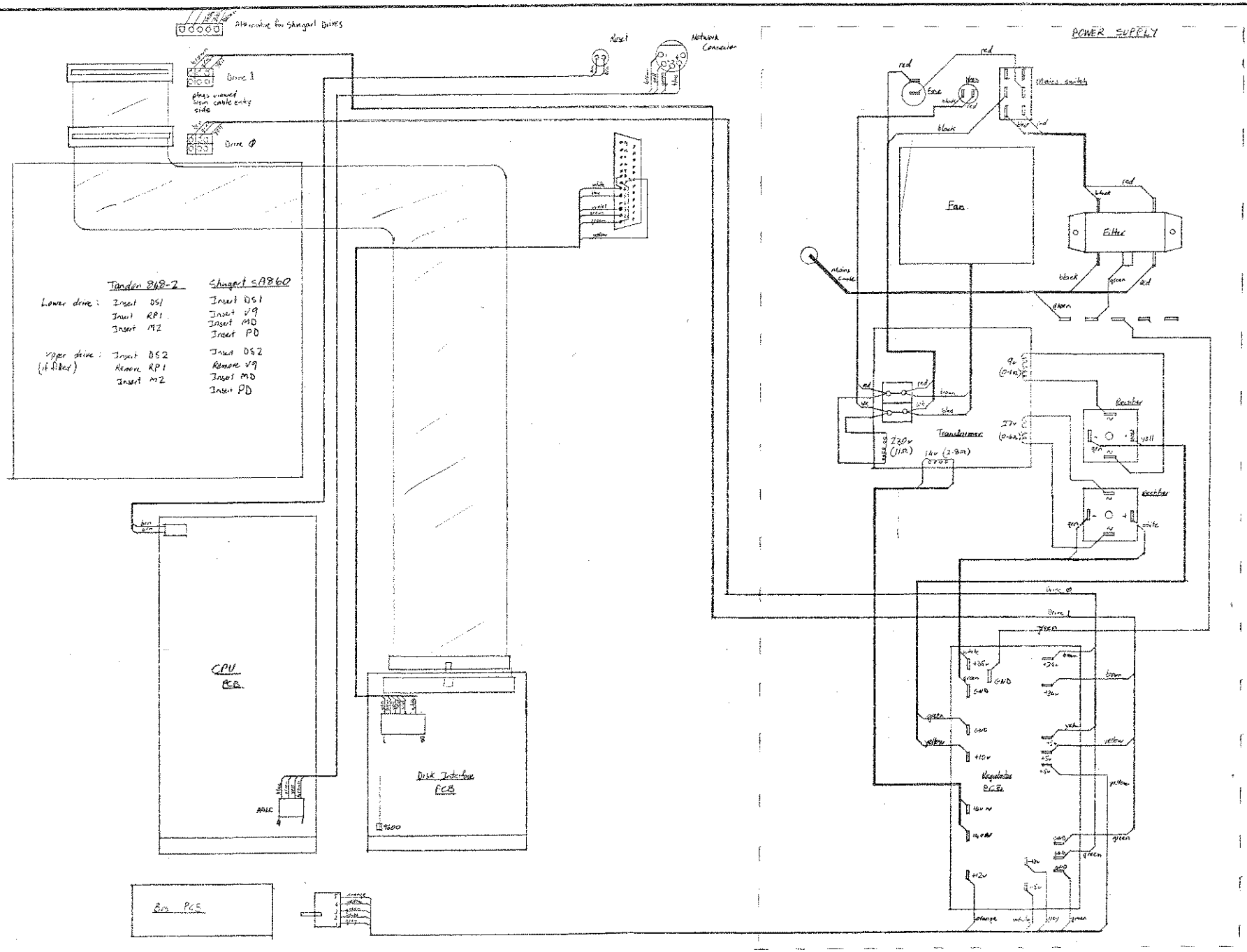
POLY DISC CONTROLLER PCB			DWG
Circuit Diagram / Component Location			200
DRAWN ICR	CHECKED	SCALES	SERIES OF
TRACED	DATE 11/11/81		REF



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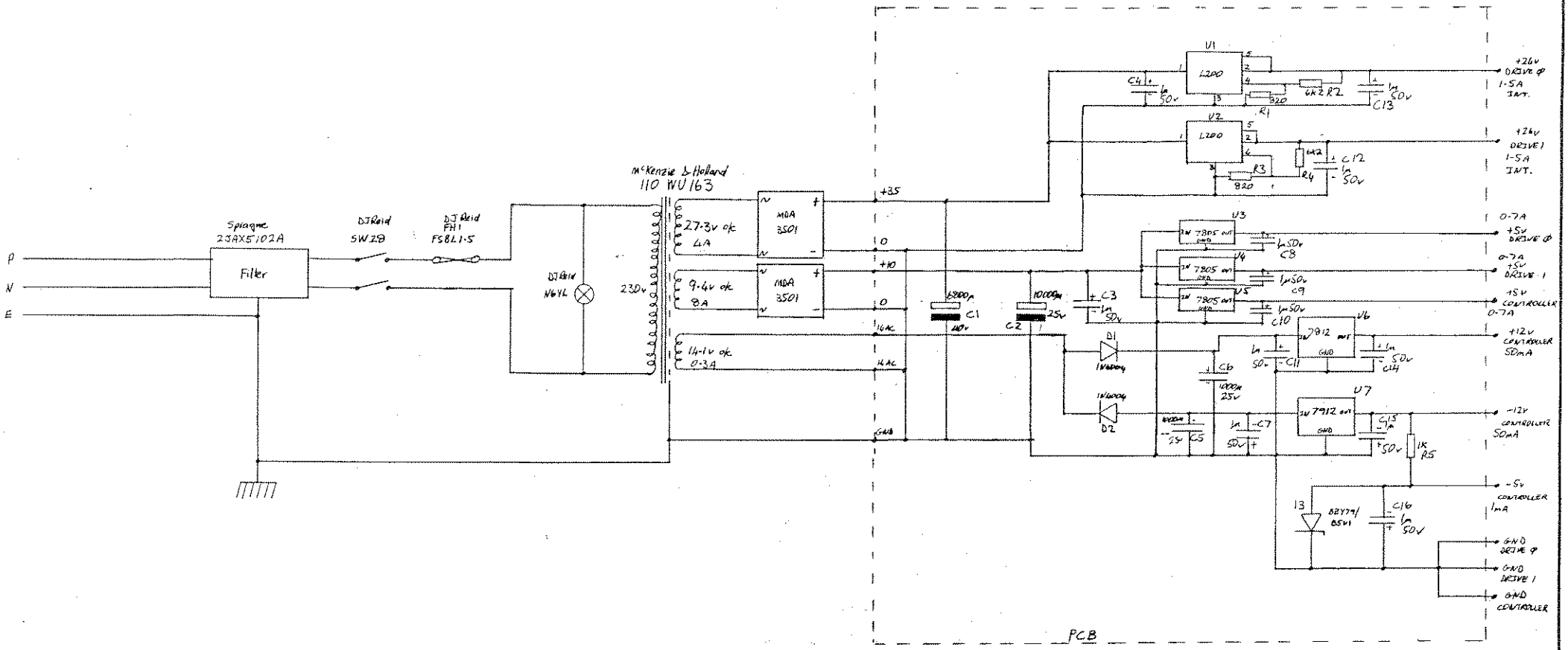
UNIVERSAL TWIN DRIVE COMPUTER

Wiring Diagram.

DRAWN	CHECKED	SCALES	SHEET
TRACED	DATE		SERIES OF
			ASP



POLYCORP

TWIN DISK UNIT
Power Supply

DRAWN	CHECKED	SCALES	SHEET
TRACED	DATE		SERIES OF
			REF