PROTEUS COMPUTER

Technical Manual

Issue 3. 11/2/85

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Contents

1. GENERAL

1.1 Specifications

Processors	6809,Z80
RAM	64 Kbytes
ROM	4 Kbytes
Clock	Z80 4 MHz (1 wait state per machine cycle) 6809 4 MHz clock, 1 MHz cycle
Disk Drives	One or two 8" half height drives (Shugart SA860) Double sided single density Capacity 630 Kbytes per disk (CP/M) 590 Kbytes (Flex,Polysys) Single sided can be used for compatibility
Ports	Standard One RS232 One Poly network Optional Total 3 RS232 One Poly network One parallel One disk drive extension

Operating Systems

CP/M. The standard operating system for 8080/Z80 micros.
FLEX. The standard operating system for 6809 micros.
POLYSYS. The operating system for the POLY network.

Size 382mm wide, 133mm high, 373mm deep

Power Requirement

230 Volts AC +-10%, Approx 140 Watts

Operating Temperature

0 C to 35 C

Operating Relative Humidity

20% to 90%, non condensing

1.2 Dual Processors.

Either the Z80 or the 6809 can be running at a given time, but not both. The two processors can however pass control to each other. The system always starts with the 6809 running and the Z80 remains reset. The 6809 reads in the first sector on the disk and starts execution of it. If it is a FLEX or POLY disk the the system operates exactly as before. If it is a CP/M disk one of the first few instuctions halts the 6809 and starts up the Z80. The rest of CP/M is then loaded and executed.

1.3 Ports.

Options are available with one RS232 port or with 3 RS232 ports and one parallel port.

1.3.1 Single Port Operation

The single port is connected to a terminal with a controlled printer port eg ADM-21. When the CP/M I/O software (BIOS) detects output to the printer it automatically sends control charaters to the terminal to select the 'transparent print' mode - and the following output is sent to the printer without being displayed on the screen. The normal mode is reselected in a similar manner when output to the screen resumes. BIOS may easily be modified to use the control codes applicable for various terminals.

Although ADM-31 and ADM-42 terminals do work in the above manner they do not handshake correctly when printing.
The terminal must be set for conversational mode,full duplex,9600 baud, 8 data bits, no parity, 1 stop bit. The printer interface on the terminal must be set to suit the printer. If an EPSON printer is used with an ADM-42 a special cable must be used which connects pin 20 of the printer to pin 19 of the ADM-42.

1.3.2 Multiple Port Operation

One port is dedicated to the terminal, one to the printer and a third RS232 port is available for connection to a mainframe etc.

A parallel port is available for connection to a Centronics-like parallel printer, or to a hard disk interface.

1.3.3 Terminal RS232 Port (Printer port for Poly system)

Address	04,05 (E004,5 for 6809)
IC	MC6850
CP/M device	CON:
Baud Rate	300,600,1200,2400,4800,9600 Selectable by jumper.
Protocol	8 data bits, no parity, 1 stop bit.(Software selectable)
Connector	D825 Female connector on PROTEUS.

Con nections-

1	: GROUND	
2	: TXDATA	Data transmitted by terminal to PROTEUS.
3	: RXDATA	Data transmitted by PROTEUS to terminal.
5	: CLEAR TO SEND	Normally high level output by PROTEUS. Can be set low by software.
6	: DATA SET READY	High level output by PROTEUS.
7	: GROUND	
8	: DATA CARRIER DETECT	High level output by PROTEUS.
20	: DATA TERMINAL READY	High level output by terminal when it is ready to receive data. No data will be transmitted by PROTEUS while this line is low.

1.3.4 Printer RS232 Port

Address	08,09 (E008,9 for 6809)
IC	MC6850
CP/M device	LST: (LPT:)
Baud Rate	300,600,1200,2400,4800,9600 Selectable by jumper.
Protocol	8 data bits, no parity, 1 stop bit.(Software selectable)
Connector	DB25 Female connector on PROTEUS.

Connections-

1	: GROUND	
2	: TXDATA	Data transmitted by printer to PROTEUS.
3	: RXDATA	Data transmitted by PROTEUS to printer.
5	: CLEAR TO SEND	Normally high level output by PROTEUS. Can be set low by software.
6	: DATA SET READY	High level output by PROTEUS.
7	: GROUND	
8	: DATA CARRIER DETECT	High level output by PROTEUS.
20	: DATA TERMINAL READY	High level output by printer when it is ready to receive data. No data will be transmitted by PROTEUS while this line is low.

The CP/M software will allow hardware handshake with pin 20 or software handshake with X-ON, X-OFF protocol.

1.3.5 Modem RS232 Port

Address	0C,0D (E00C,D for 6809)
IC	MC6850
CP/M device	RDR:, PUN:
Baud Rate	300,600,1200,2400,4800,9600 Selectable by jumper.
Protocol	8 data bits, no parity, 1 stop bit.(Software selectable)
Connector	DB25 Female connector on PROTEUS.

Connections-

1	: GROUND	
2	: TXDATA	Data transmitted by PROTEUS to modem.
3	: RXDATA	Data transmitted by modem to PROTEUS.
4	: REQUEST TO SEND	High level transmitted by PROTEUS when it wants to transmit data.
5	: CLEAR TO SEND	High level transmitted by modem when it is ready for PROTEUS to transmit data.
7	: GROUND	
8	: DATA CARRIER DETECT	High level output by modem.
20	: DATA TERMINAL READY	High level output by PROTEUS.

1.3.6 Parallel Port (Optional printer port)

Address		00-03 (E000-E003 for 6809)
IC		MC6821
CP/M Device		LST: (UL1:)
Protocol		Centronics Standard
Connector		Amphenol 57F-36 , female on PROTEUS
Pins		
1	STROBE	Low signal to indicate valid data on pins 2-9
2-9	DATA 1-8	Data
11	BUSY	High signal output by printer to when it is not ready to receive data.
16	LOGIC GND	
19-30	LOGIC GND	

All I/O pins of the 6821 are available for connection to a peripheral if required.

1.3.7 Network Port.

HDLC Port for network of POLY computers.
5 pin NEUTRICK microphone connector. Male connector on PROTEUS.

- Pin 1 : Data out from PROTEUS.
- Pin 2 : Clock out from PROTEUS.
- Pin 3 : Ground.
- Pin 4 : Data in to PROTEUS

1.4 Disks.

The normal CP/M format used is single density, double sided. 512 byte physical sectors are used with code to block and deblock the 128 byte logical sectors of CP/M. Single sided with 128 byte sectors can be used on drive B: for transfer to other CP/M systems. This format is automatically selected when a warm or cold start is performed with a single sided disk is inserted. It is considered that the double sided blocked format will always be used, except for interchange with other CP/M systems.
With FLEX and POLYSYS single or double sided need only be defined at the time of formatting the disk. 256 byte sectors are used.

1.4.1 Disk capacity.

	FLEX-POLYSYS	CP/M
Sides	2	2
Tracks/side	77	77
Sectors/track	15	8
Bytes/sector	256	512
Total formatted capacity/disk	591360	630784

In both systems the sectors on side 2 are numbered as a continuation of the sectors on the same track on side 1.

1.5 Polycorp Utilities

Utility programs have been written to format disks, check newly formatted or used disks for CRC errors, copy an entire disk onto another, etc.

The Polycorp utilities are in the file UTE.COM which displays a menu of the available commands. The command file PUTSYS should be used to copy the operating system onto a disk and to reconfigure it if necessary.

The standard CP/M utilities all operate as described in the CP/M manual except that PUTSYS should be used rather than SYSGEN. The only device assignment that can be performed with the STAT command is to select either a serial printer (LST:=LPT:) or a parallel printer (LST:=UL1:).

1.6 CP/M Software

In addition to the operating system itself the following software has been tested with complete success on the CP/M system-

MBASIC	Microsoft Basic ver 5 for CP/M
MACRO-80	Microsoft 8080 / Z80 Macro Assembler
LINK	Linking loader
ZSID	Z80 symbolic debugger
WORDMASTER	Screen editor
WORDSTAR	Word processor
MULTIPLAN	Spreadsheet calculator
DBASE-2	Database management

Notes:

1. Wordstar and Macro-80 are infinitely better than ED and ASM, the editor and assembler supplied with CP/M.
2. If an ADM-21 terminal is used with Wordstar be sure that it has the 4k Z8 fitted. With the initial 2k it was far too slow. When installing Wordstar select ADM-31 for ADM-21, ADM-31, ADM-42 and Televideo 910+. LST: will always work for the printer, but to allow simultaneous printing and editing with a multiport Proteus it is better to use Wordstars port driver.

1.7 Low-level CP/M programming notes

Interupts are not normally used in the CP/M system. If they are required the Z80 must be programmed for Interupt Mode 1. A jump instruction to the interupt service routine must then be inserted at address 0038H. Note that this restart is the same as that normally used by the debugger ZSID for breakpoints and tracing - however ZSID can be patched to use another restart.

If it is required to use the timer chip in the Z80 mode it should be noted that the E input which is 1MHz in the 6809 mode will not be a constant frequency. However a fixed 1MHz signal has been connected to the external clock inputs of the timer and it should be programmed to use that.

1.8 Memory maps

In the Z80 mode the I/O ports are shifted to the Z80 I/O space and the EPROM is deselected. This gives 64k of RAM.

FLEX memory map

Address	Type	Contents
0000	RAM	User RAM (Large transient progs)
BFFF		
C000	RAM	FLEX operating system
DFFF		(Small transient programs)
E000-3		PIA - 6821 (Parallel port)
E004-5	I/O	ACIA - 6850 (Terminal)
E008-9		ACIA - 6850 (Printer)
E00C-D		ACIA - 6850 (Modem)
E014		Drive register
E018-B		FDC - 1771 (Floppy control)
E020-7		PTM - 6840 (Timer)
E030-6		ADLC - 6854 (Poly network)
E060		Enable Z80
F000	ROM	BOOTSTRAP,6809 DEBUGGER ETC
FFFF		

CPM memory map

Address	Type	contents
0000	RAM	CPM Variables etc
00FF		
0100	RAM	TPA
DFFF		(Transient Program Area)
E000	RAM	CCP
E7FF		(Console command processor)
E800	RAM	BDOS
F5FF		(Basic Disk Operating System)
F600	RAM	BIOS
FFFF		(Basic Input-Output System

CPM I/O MAP

00-03	PIA - 6821	(Parallel port)
04-05	ACIA - 6850	(Terminal)
08-09	ACIA - 6850	(Printer)
0C-0D	ACIA - 6850	(Modem)
14	Drive register	
18-1B	FDC - 1771	(Floppy controller)
20-27	PTM - 6840	(Timer)
30-36	ADLC - 6854	(Poly network)
50	Enable 6809	

2.0 Z80-6809 Processor PCB

2.1 General Description

U7,U8 are the two microprocessors.Their address and data busses are connected in parallel, and it is arranged so that when each one is operating the other is in a high impedance state.

U10,U11,U33 are used to generate timing signals from the Z80 which more or less correspond to those generated by the 6809.

U25,U26 select the control and I/O decode signals from the 6809 or the Z80, depending on which is running.

U27 decodes the memory addresses in the E000-EFFF range in the 6809 mode and decodes the I/O port addresses in the Z80 mode. It should be noted that the decoded signals are disabled during the first part of any machine cycle (when the address lines are all changing) so that glitches do not occur on the outputs.

U28 is the disk bootstrap and debug ROM. It is accessible only in the 6809 mode.

U30 is used to keep time of day and to generate the clock signal for the network only when running POLYSYS.

U30 is the data link control IC.

U12-U19 are the 64k x 1 dynamic memories.

U22 is the refresh counter. As an 8 bit refresh address is generated, memory ICs which require 7 or 8 bit refresh addresses can be used.

U20,U21 select the refresh address instead of the CPU address during the refresh operations.

U23,U24 are the row/column address multiplexor used to multiplex the 16 bit CPU address onto the 8 address pins of the memory ICs.

2.2 Operation of Dual Processors

The simplified operation of the dual processor is as follows- The control signals required for the memory and I/O are generated by the 6809 more or less directly. The Z80 control signals are manipulated so that they approximate those generated by the 6809. A data selector is then used to select the source of the control signals for the rest of the system depending on which processor is running.

2.3 Clock Oscillator

A 4MHz oscillator (U4,X1,Q1) is used to drive the clock inputs of both the 6809 and Z80. This results in the 6809 operating at a (bus) frequency of 1MHz. One wait state is inserted into each machine cycle of the Z80 to reduce its bus frequency to approximately 1MHz also.

2.4 Generation of control signals

With the 6809 in control RAS is activated when Q goes high. The address lines of the memory chips are switched when E goes high. CAS is activated when Q goes low. Finally when E goes low the cycle is complete and RAS and CAS are de-activated. Refresh of the memory occurs during cycles when E000 or above is addressed ie I/O, ROM or internal operations. RAS is generated as above but CAS is not generated. Instead of the CPU address being selected the refresh counter is selected during the entire refresh cycle and incremented at the end of the cycle.

With the Z80 in control RAS is activated on the first positive clock edge after MREQ is activated. This is also the start of the wait state. The address lines are switched on the next negative edge of the clock. CAS is then activated on the next positive edge of the clock. At the end of MREQ, RAS and CAS are both de-activated. Refresh occurs during the RFSH output of the Z80 which is used to select the refresh counter and to increment it. RAS is generated by U11a during the refresh operation.
The control signals are generated in a similar manner during I/O cycles. RAS is also generated on the first positive clock edge after IOREQ is asserted. (This refreshes a random memory address!) On the folowing negative clock edge "E" is generated as required by the 6800 family peripherals. "E" is also generated during memory cycles as it is the same signal as the multipexor control.

2.5 Transfer of control

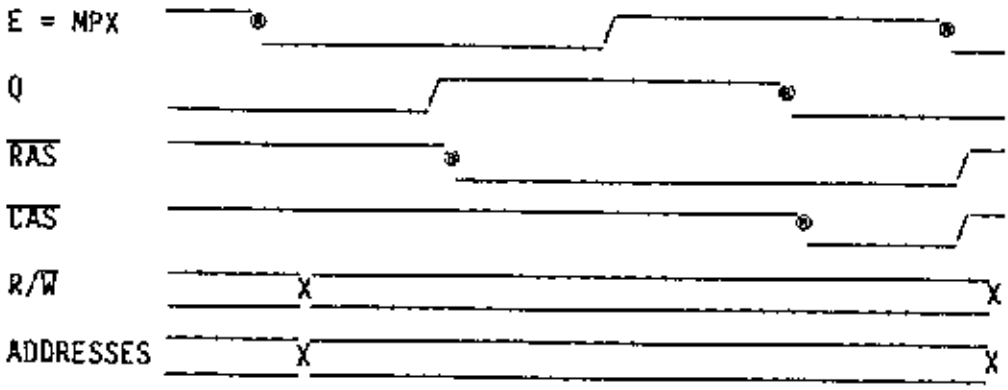
When the PCB is reset the 6809 is always selected. To transfer control to the Z80, the 6809 should execute a double byte store instruction to $E060. This will halt the 6809 at the end of the instruction and at the same time remove the reset from the Z80. After a couple of clock cycles the Z80 will start execution of the instruction at 0000. This instruction must have been put there by the 6809.

To transfer control back to the 6809, the Z80 should execute an output to I/O port 50. This will immediately reset the Z80 and the 6809 will continue operation with the instruction following the double byte store insruction which it used to halt itself.

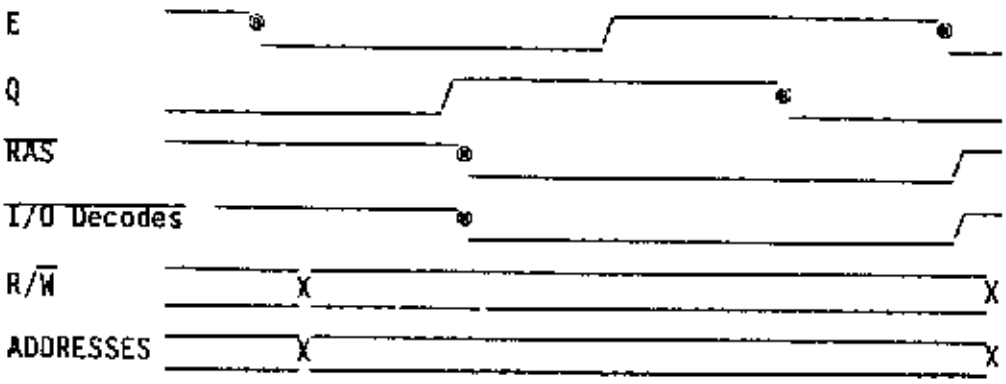
It should be noted that when the switch is made from one set of control signals to the other, by altering the state of the select input to U25,U26, that all of the control signals are always inactive.

2.6 6809 Timing Diagram

Memory cycle

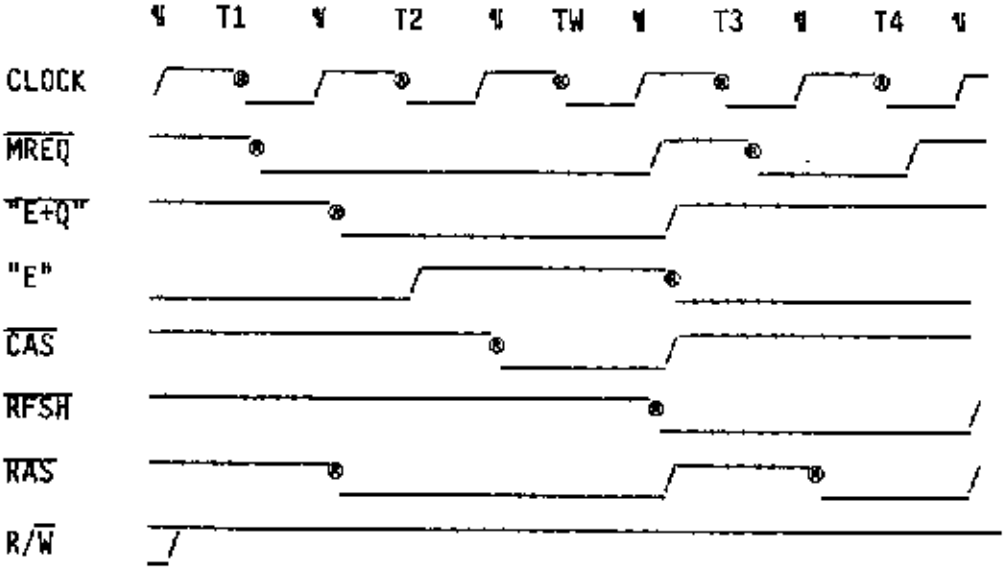


I/O cycle

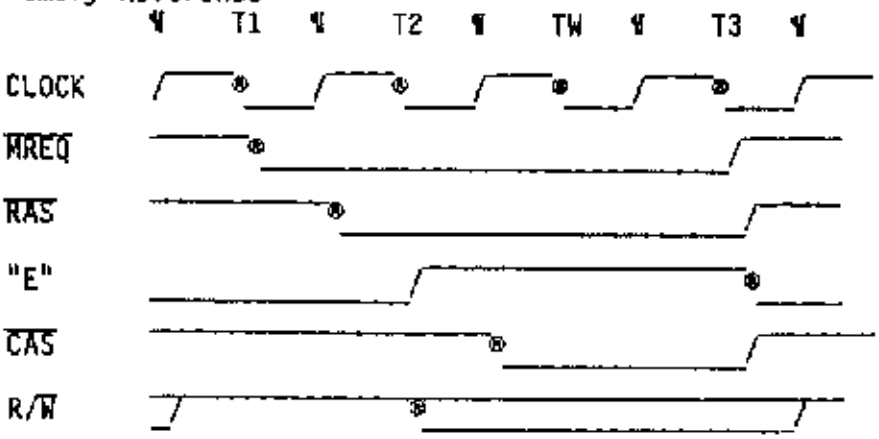


2.7 Z80 Timing Diagram

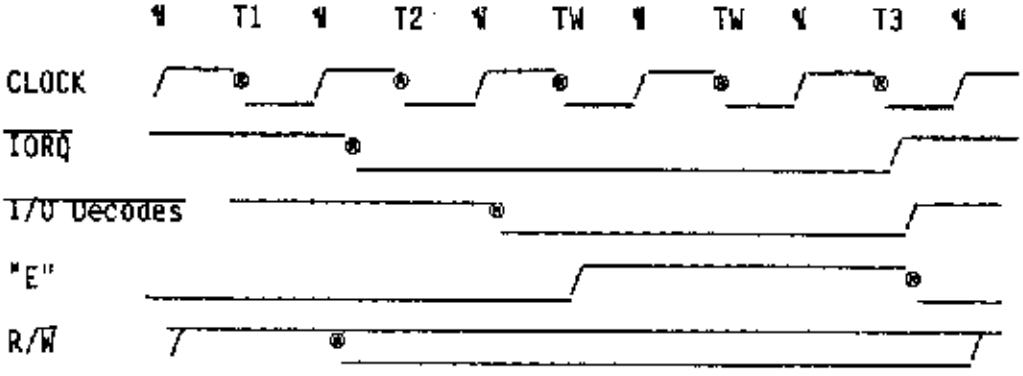
Instruction Fetch



Memory Reference



I/O Cycle



3.0 Disk Controller PCB

3.1 General

U12 is the floppy disk controller IC which performs most of the fuctions required for the floppy disk interface.

U15 is the inverting data bus buffer used to connect the logic true bus of the CPU to the logically inverting data bus of the floppy disk controller IC.
U7 is the drive and side select register.

U16 is used to enable the drive select signals for 3 seconds after any CPU access to the disk controller.

U1,U3,U4 are the driver ICs for the disk drive interface.

U5 is the receiver IC for the disk drive interface.

U13,U17,U9,U10 are the data separator circuit.

U19 is the ACIA ie interface for the serial RS232 interface.

U6,U11 are the driver and receiver ICs for the RS232 interface.

U14,U18 are the baud rate generator for U19.

3.2 Drive and side select

Address E014 (I/O port 14) is the write-only drive select register. The lower 2 bits define the drive-

00 = drive 0 or A
01 = drive 1 or B

Other codes are invalid as there are only two drives.
Bit 6 is the side-select control-

0 = side 1 (or 0!)
1 = side 2 (or 1!)

The drive selects are enabled for approximately 3 seconds after the last disk access. After the disk has not been accessed for this time, all drives will be deselected. The SHUGART Drives normally used will remain on for 3 seconds after this, after which the red indicator is extinguished and the door lock released. The TANDON drives optionally fitted will immediately extinguish their red indicator but remain turning for 30 seconds after this time after which their motors are stopped.

3.3 Disk Change Detector

The Disk-change output from the selected drive can be read by the CPU reading location E014 bit 1. If it is a 1, the disk drive door has been opened since the drive was last selected. This bit is cleared when the drive is deselected.

3.4 Floppy disk controller

The FD1771 IC performs all the reading, writing, and head stepping functions required by the floppy disk system. For more

information the manufacturers data sheet should be consulted.

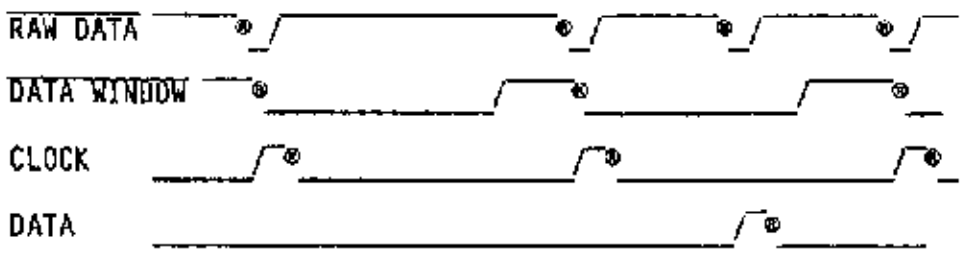
3.5 Data Separater

The output from the drive consists of clock pulses (nearly) every bit boundary (every 4 microseconds), and data pulses midway between the clock pulses if the data bit is a 1. If the data bit is a 0 there is no data pulse.
The data separater basically consists of a 3 microsecond monostable triggered by the clock pulses. If another pulse arrives during this time it is considered to be a data pulse. The data and clock pulses are routed to separate inputs of the 1771.
This simple operation is complicated by the fact that during address marks and other special marks on the formatted disk there are missing clock pulses used to identify the special marks. When this happens U13a, which is triggered by data pulses, is used to trigger U13b at around the time that it would normally be triggered by a clock pulse. At the end of 3 consequeutive missing clock pulses, U21 pin 6 goes low which resets the monostable and determines that the next pulse will be taken as a clock pulse. This normally happens during the special marks and also if the separater starts off with the data and clock pulses around the wrong way.
U10c and U10d are used to ensure that a change in the data window generated by U13b cannot take effect during a data or clock pulse.

3.6 Data separater alignment

1. Load the head on a formatted disk.
2. Monitor U10 pin 12 with an oscilloscope and adjust RV1 until the length of the negative going pulses is 3.0 microseconds.
3. Monitor U17 pin 11 with the oscilloscope and adjust RV2 until the bright negative going pulse PLUS the dim extension is 2.7 microseconds.

3.7 Data separater timing diagrams



4.0 I/O PCB

This PCB also functions as the bus PCB to connect the processor PCB and the disk interface PCB.

U2 is the ACIA (Asynchonous Communications Interface Adapter) for the modem port. U7 and U8 provide translation to RS232 levels. Note that this port is wired for direct connection to a modem ie for connection to "data set equipment".

U3 is the ACIA for the printer port. U8 and U9 provide translation to RS232 levels. Note that this port is wired for direct connection to a printer ie for connection to "data terminal equipment". Jumper J3 can be used to select between a high READY handshake signal or a high BUSY handshake. Most printers use pin 20 (DTR) as a high READY signal.

U4 is the PIA (Peripheral Interface Adapter) for the parallel printer port or hard disk interface. This is connected for use with a Centronics type interface, however all the pins are taken out to facilitate connection to other devices.

U5 and U6 provide 16 times a selection of baud rates from 300 to 9600 and the baud rate for the modem may be selected with J1 and the rate for the printer may be selected with J2.

5.0 Power Supply

The power supply is a conventional transformer/ capacitor input filter/ linear regulator design. The transformer has 3 windings-

1. 27.3 Vac (used for 24v dc)
2. 9.4 Vac (used for 5v dc)
3. 14.1 Vac (used for +12v,-12v,-5v dc)

The regulator assembly produces the following supplies for EACH drive-
+24v +- 10% at 1.5 A intermittent
+5v +- 5% at 0.7 A

and the following supplies for the computer and interface PCBs
+12v +- 10% at 50mA
+5v +- 5% at 0.7 A
-5v +- 10% at 1mA
-12v +- 10% at 50mA

The power supply is capable of maintaining the above outputs with a mains voltage of 200-260 volts.

6.0 Production Testing

The CPU board and disk interface board are tested with the EXORCISOR plugged into the 6809 socket using the program MIN164. This tests most of the board except for the Z80 associated components.
If the boards pass the above test it should be able to boot FLEX. The Z80 circuitry can then be tested with the program Z80-6809. The memory should then be tested with the program MTEST64. The disk drives should then be checked by copying the complete contents of a disk onto the other drive and back again using the FLEX MIRROR command. Finally it should be verified that CP/M will run by booting a CP/M disk.

REFERENCE	PART CODE	QTY
AIR FILTER	AIR FILTER	1.00
DISK POWER CONNECTOR	AMP 1-480270-0	2.00
PINS FOR DISK POWER CONNECT	AMP 0-160304-2	6.00
FASTON TERMINALS	FASTON RED	42.00
RS232 CONNECTORS	AMPH 17-304-01	1.00
PINS FOR RS232	AMPH 17-763-02	9.00
SCREW SOCKET (SET OF TWO)	AMPH 17-893	1.00
FRONT TRIDENT & 'PROTEUS'.	BADGE PROTEUS	1.00
MULTICORE 7 (DECIMETRES)	CABLE 7 CORE ELV	1.00
CABLE TIES	CABLE TIE 200MM	20.00
DWG 610	CHASSIS PROTEUS	1.00
PROT SHIPPING CONTAINER	CARTON PROTEUS	1.00
MAINS CORD & TAPON. MOULDED	CORDSET MAINS	1.00
DWG 620	COVER PROTEUS	1.00
FUSE HOLDER	DAVRED FH1	1.00
FUSE	DAVRED FS3L1	1.00
HEAT SINK FOR TRANSISTOR	DAVRED HS57	1.00
CABLE ANCHOR	CORD GROMMET LARGE	1.00
CLIP FOR NEON	DAVRED N4	1.00
WASHER FOR NEON	DAVRED N6	1.00
NEON INDICATOR	DAVRED N6YL	1.00
RESET SWITCH	DAVRED SW16	1.00
MAINS SWITCH	DAVRED SW20	1.00
HOOKUP WIRE 0.5MM	DAVRED WIF19	1.00
HOOKUP WIRE 0.6MM	DAVRED WIL03	2.00
SCREWS FOR DRIVE	SCREW US 8*32*0.5"	8.00
PCB MTG EXTRUSION	EXTRUSION SHORT	2.00
MAINS FILTER	FILTER 230V 6A	1.00
GROMMETS FOR I/O BOARD	GROMMET #2	4.00
FAN	FAN	1.00
TERMINALS FOR 3001 SERIES	MOLEX 2478-SL1	5.00
TERMINALS FOR 6471 SERIES	MOLEX 2759-01L	17.00
DC POWER CABLE HOUSING	MOLEX 3001-5	1.00
RESET SWITCH CONNECT HSG	MOLEX 2695-02R	1.00
NETWORK CONNECT HOUSING	MOLEX 2695-04R	1.00
RS232 CABLE HOUSING	MOLEX 2695-09R	1.00
JUMPER FOR DRIVE OPTIONS	MOLEX 7959-02-SP0	6.00
NETWORK CONNECTOR	NETWORK MOD??	1.00
MISC NUTS	NUT M3	16.00
NUTS FOR AIR FILTER	NUT M3 NYLOC	4.00
FOR I/O BOARD	NUT M3 NYLOC	4.00
FOR TRANSISTOR	NUT M3 NYLOC	1.00
MISC NUTS	NUT M4	14.00
MISC NUTS	NUT M4 NYLOC	4.00
LABELS	LABEL PROTEUS	1.00
FOR WIRING HARNESS	P CLIP	3.00
TERMINAL STRIP	CONNECTOR BLOCK	9.20
RUBBER FEET	FEET PLASTIC	4.00
TO220 INSULATING PAD	PAD TN3U TO220	1.00
RECTIFIER	RECT MDA3501	2.00

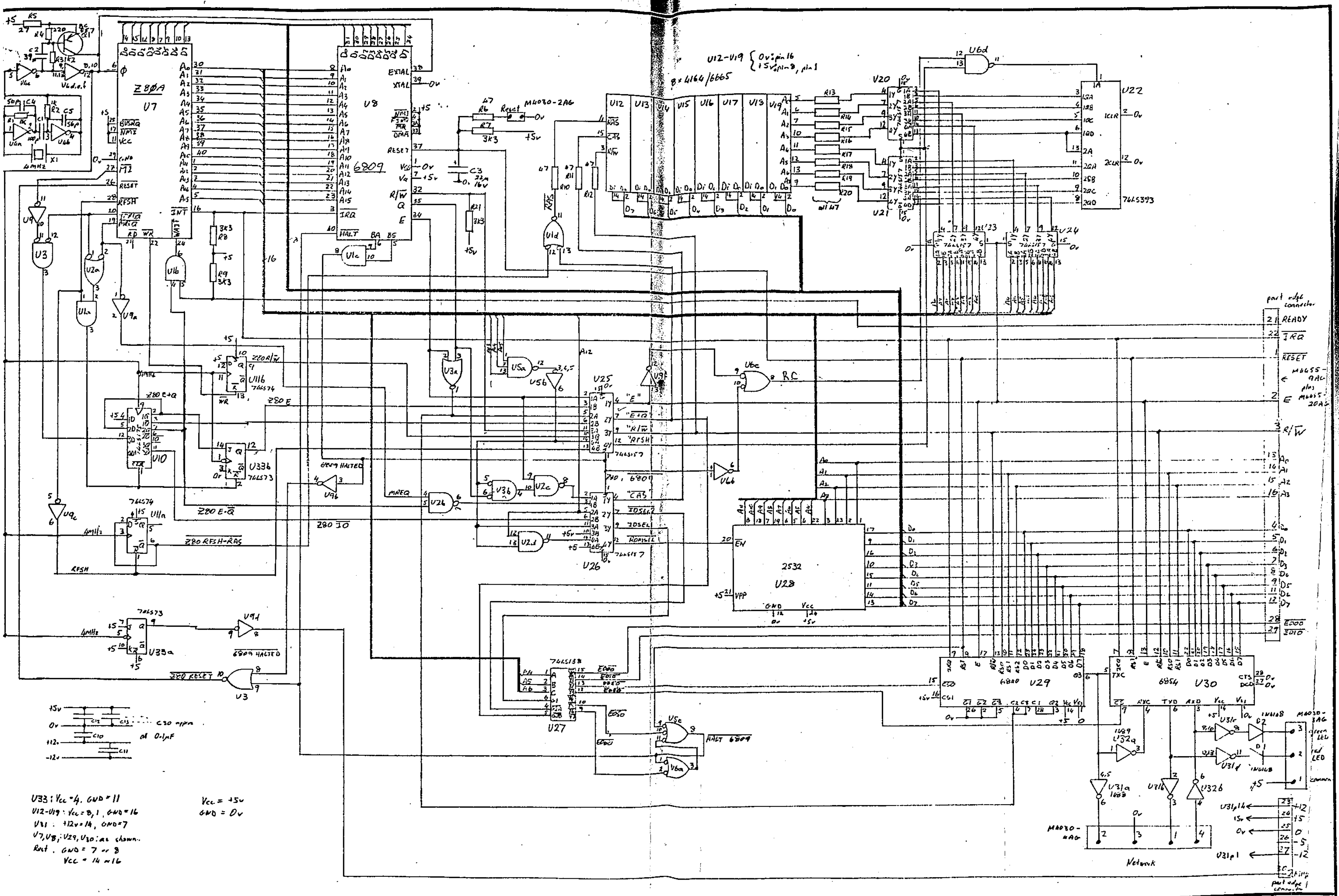
REFERENCE	PART CODE	QTY
RIBBON CABLE 50 WAY	RN CAB-50	2.00
CONNECTOR TO DRIVE PCB	RN IDE-50	2.00
CONNECTOR TO DISK CONT PCB	SKT 50PIN STANDARD	1.00
POLARISATION KEY FOR DRIVES	RN PK-2	2.00
FOR FAN	SCREW M3*12	4.00
-ON TERM STRIP	SCREW M3*16	2.00
FOR I/O BOARD	SCREW M3*16	4.00
FOR CKTS,PSU	SCREW M3* 8	11.00
FOR TRANSISTOR	SCREW M3* 8	1.00
FOR PSU TO CHASSIS	SCREW M4*10	10.00
FOR FEET	SCREW M4*16	4.00
SCREW FOR BRIDGE RECT	SCREW M4*20	2.00
XFMR,CASE,FLTR,2 MIS PLATES	SCREW M4* 6	14.00
TRANSISTOR INSULATING PAD	STLP40 400.TIP PAC	1.00
TRANSISTOR FOR +24V TO DRIVES	TRANSTR TIP35C	1.00
EARTH LUGS	UTILUX 1944	5.00
MISC WASHERS	WASHER M3 STAR	16.00
MISC WASHERS	WASHER M4 STAR	14.00
TRANSFORMER	XFMR PROTEUS	1.00
QUALITY ASSURANCE LABEL	LABEL Q/A	2.00

REFERENCE	PART CODE	QTY
U4	IC 74LS04	1.00
U2,U3	IC 6850	2.00
U1	IC 6821	1.00
U5	IC 74LS191	1.00
U6	IC 74LS393	1.00
U7,U9	IC 14894	2.00
U8	IC 1489	1.00
P1	MOLEX 2599-5AG	1.00
P2,P4	MOLEX 4030-09AG	2.00
P3,P5	MOLEX 4030-20AG	2.00
P6,P7	MOLEX 6373-08AG	2.00
J1,J2,J3	MOLEX 4030-03AG	7.00
R1-R6	RES 3K3 .6W	6.00
P8	HEADER 34PIN STR	1.00
JUMPERS	MOLEX 7809-02-5/0	3.00
PCB	PCB I/O PROTEUS	1.00
RS232 CONNECT	AMPH 17-304-01	2.00
RS232 HOUSING	MOLEX 7695-08R	2.00
0.1" TERMINAL	MOLEX 2759-01L	21.00
EXTENSION DRIVE CONNECT	AMPH 57F-40500	1.00
PARALLEL PORT CONNECT	AMPH 57F-40360	1.00
CONNECT TO PCB	SKT 34PIN STANDARD	1.00
34 WAY RIBBON CABLE	RN DAB-34	1.60
SCREW SOCKET (SET OF TWO)	AMPH 17-B93	2.00
PINS FOR RS232	AMPH 17-763-02	16.00
FOR U1	SKT 40 PIN DIL	1.00
FOR U7-U9	SKT 14 PIN DIL	3.00
EJECTORS FOR P8	RN EL-2K	2.00
SCREWS FOR PARALLEL,EXTN SKTS	SCREW M3*10	4.00
SCREWS FOR PCB MTG	SCREW M3*12	4.00
MISC NUTS	NUT M3	8.00
MISC NUTS	NUT M3 NYLOC	4.00
MISC WASHERS	WASHER M3 STAN	8.00
MISC WASHERS	WASHER M3 FLAT	4.00
QUALITY ASSURANCE LABEL	LABEL Q/A	1.00

REFERENCE	PART CODE	QTY
U12	IC 1771	1.00
U19	IC 6850	1.00
U16	IC 4538	1.00
U6	IC 1488	1.00
U11	IC 1489A	1.00
U9,U10	IC 74LS00	2.00
U8	IC 74LS04	1.00
U2	IC 74LS08	1.00
U5	IC 74LS14	1.00
U1,U3,U4	IC 7438	3.00
U17,U21	IC 74LS74	2.00
U20	IC 74LS138	1.00
U7	IC 74LS175	1.00
U18	IC 74LS191	1.00
U13	IC 74LS221	1.00
U14	IC 74LS393	1.00
U15	IC 74LS640	1.00
SOCKET U6,U11	SKT 14 PIN DIL	2.00
SOCKET U19	SKT 24 PIN DIL	1.00
SOCKET U12	SKT 40 PIN DIL	1.00
C2,C3	CAP 100P 63V	2.00
C1 + DECOUPLING	CAP 100N 63V	14.00
C4	CAP 1U 50V TAN	1.00
R1-R6	RES 150R .6W	6.00
R13	RES 470R .6W	1.00
R7	RES 3K3 .6W	1.00
R11	RES 22K .6W	1.00
R12	RES 680R .6W	1.00
R10	RES 5K3 .6W	1.00
R9	RES 27K .6W 1%	1.00
R8	RES 33K .6W 1%	1.00
RV1,RV2	POT 20K CERMET	2.00
CONNECT TO RS232	MOLEX 6373-09A6	1.00
BAUD RATE SELECTOR PINS	MOLEX 4030-14A6	1.00
BAUD RATE JUMPER	MOLEX 7859-02-5P0	1.00
EDGE CONNECTOR	MOLEX 4455-10P6	1.00
EDGE CONNECTOR	MOLEX 4455-20P6	1.00
POLARIZING PIN	MOLEX 4161-01	1.00
CONNECT TO DRIVE	HEADER 5CPIN RHT	1.00
EJECTORS	RN EL-2K	2.00
PCB	PCB DISK CONTROLLR	1.00
QUALITY ASSURANCE LABLL	LABEL QA	1.00

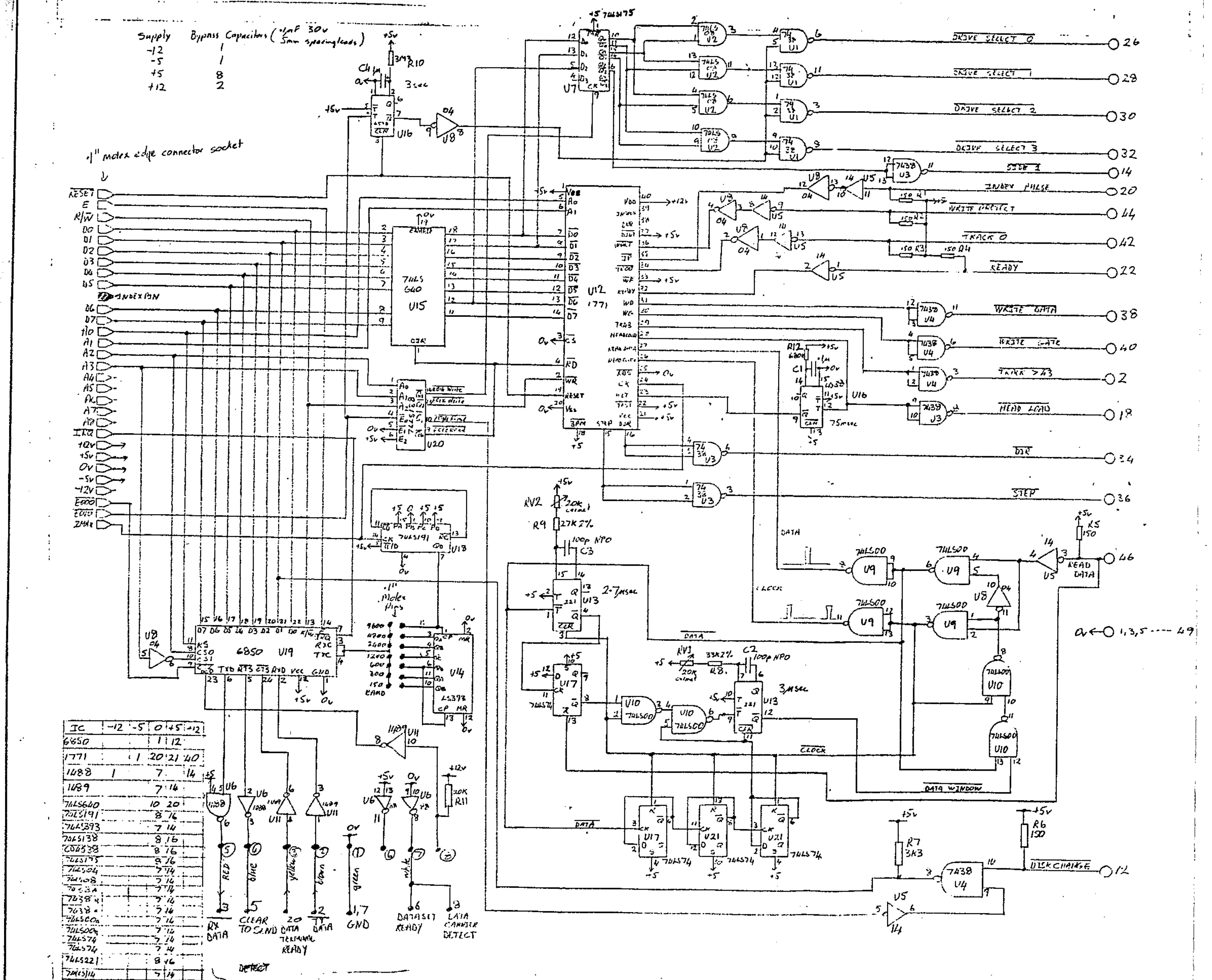
REFERENCE	PART CODE	QTY
U1	IC 74LS08	1.00
U2,U6	IC 74LS00	2.00
U3	IC 74LS02	1.00
U4,U9	IC 74LS04	2.00
U5	IC 74LS10	1.00
U7	IC Z80A-CPU	1.00
U8	IC 6809	1.00
U10	IC 74LS175	1.00
U11	IC 74LS74	1.00
U12-U19	IC MSK 4164 P-20	8.00
U20,U21,U23,U24,U25,U26	IC 74LS157	6.00
U22	IC 74LS393	1.00
U27	IC 74LS138	1.00
U28	IC 2532	1.00
U29	IC 6840	1.00
U30	IC 6854	1.00
U31	IC 1488	1.00
U32	IC 1489A	1.00
U33	IC 74LS73	1.00
SOCKETS U31,U32	SKT 14 PIN DIL	2.00
SOCKETS U12 - U19	SKT 16 PIN DIL	8.00
SOCKET U28	SKT 28 PIN DIL	1.00
SOCKET U29,U30	SKT 28 PIN DIL	2.00
SOCKET U7	SKT 40 PIN DIL	1.00
SOCKET U8	SKT 40 PIN SPUN	1.00
R1,R2	RES 1K .6W	2.00
R3	RES 1K2 .6W	1.00
R4	RES 220R .6W	1.00
R5	RES 27R .6W	1.00
R6,R10-R20	RES 47R .6W	12.00
R7,R8,R9,R21	RES 3K3 .6W	4.00
Q1	TRANSTR BC557	1.00
X1	XTAL 4MHZ	1.00
C1	CAP 100P 63V	1.00
C2	CAP 39P 63V	1.00
C3	CAP 22U 16V ELC	1.00
C4,C5	CAP 56P 63V	2.00
C10-C44	CAP 100N 63V	35.00
D1,D2	DIODE 1N4148	2.00
RESET CONNECTOR	MOLEX 6373-02AG	1.00
LED CONNECTOR	MOLEX 4030-03AG	1.00
NETWORK CONNECTOR	MOLEX 6373-04AG	1.00
EDGE CONNECTOR	MOLEX 4456-104G	1.00
EDGE CONNECTOR	MOLEX 4455-204G	1.00
POLARIZING PIN	MOLEX 4161-01	1.00
PCB	PCB CPU PROTEUS	1.00
QUALITY ASSURANCE LABEL	LABEL Q/A	1.00

REFERENCE	PART CODE	QTY
U1	IC L200CV	1.00
U3, U4, U5	IC 7805A	3.00
U6	IC 7812	1.00
U7	IC 7912	1.00
D1, D2	DIODE 1N4004	2.00
D3	DIODE BZY79/B5V1	1.00
C1	CAP 6800U 40V	1.00
C2	CAP 10000U 25V	1.00
C5, C6	CAP 1000U 25V PCB	2.00
C3, C4, C7-C16	CAP 1U 50V T4N	12.00
R2	RES 6K2 .6W 1%	1.00
R1	RES 820R .6W 1%	1.00
R3	RES 1K .6W	1.00
PCB	PCB PSU PROTEUS	1.00
LUGS	PCB QC TAB	18.00
SCREWS FOR LARGE CAPACITORS	SCREW M5*8 CHEESE	2.00
QUALITY ASSURANCE LABEL	LABEL Q/A	1.00

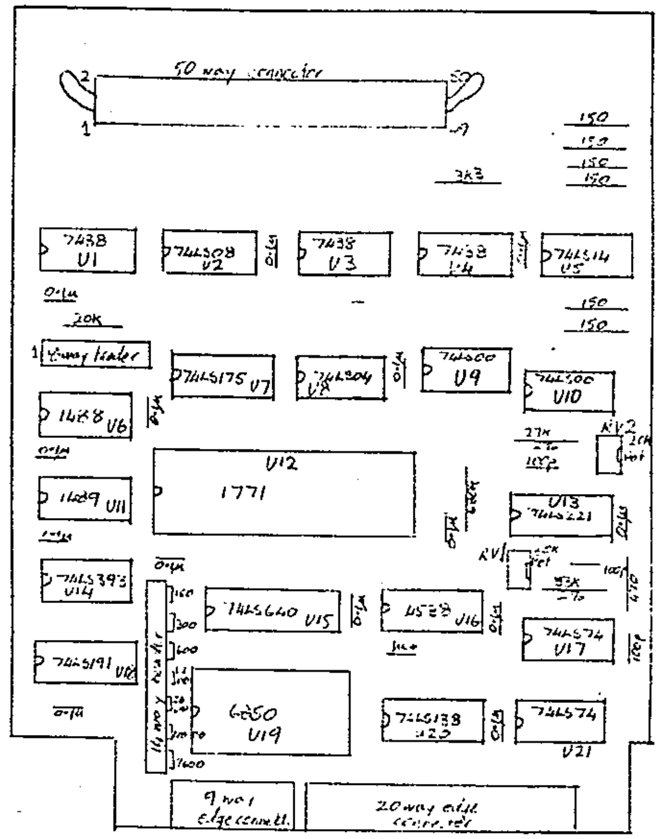


Amendments	PROTEUS PROCESSOR BOARD Z80 /6809 PROCESSOR		SHEET DWG 3880
22/7/83 ILR 13/8/84 WHM 11/2/85 ILR C.O. 6134	DRAWN ILR TRACED ILR	CHECKED ILR DATE 1/9/82	SCALES	SERIES OF REF

POLYCORP



IC	-12	-5	0	+5	+12
6850			1	12	
1771		1	20	21	40
1488	1		7		14
1489			7	14	
74LS640			10	20	
74LS191			8	16	
74LS393			7	14	
74LS138			8	16	
CD4538			8	16	
74LS175			8	16	
74LS04			7	14	
74LS08			7	14	
74LS3A			7	14	
7438 a			7	14	
7438 b			7	14	
74LS00a			7	14	
74LS00b			7	14	
74LS74			7	14	
74LS74			7	14	
74LS221			8	16	
74(LS)14			7	14	



Note: Timing Adjustment Procedure

(1) Load head using Exerciser test prog.
(2) Monitor U10 pin 12 and adjust RV1 for negative going pulses of length 3µsec
(3) Monitor U17 pin 11 and adjust RV2 for negative pulses of length 2·7µsec. Ignore the bright trace - pulse length = 4µsec - and use the dim trace.

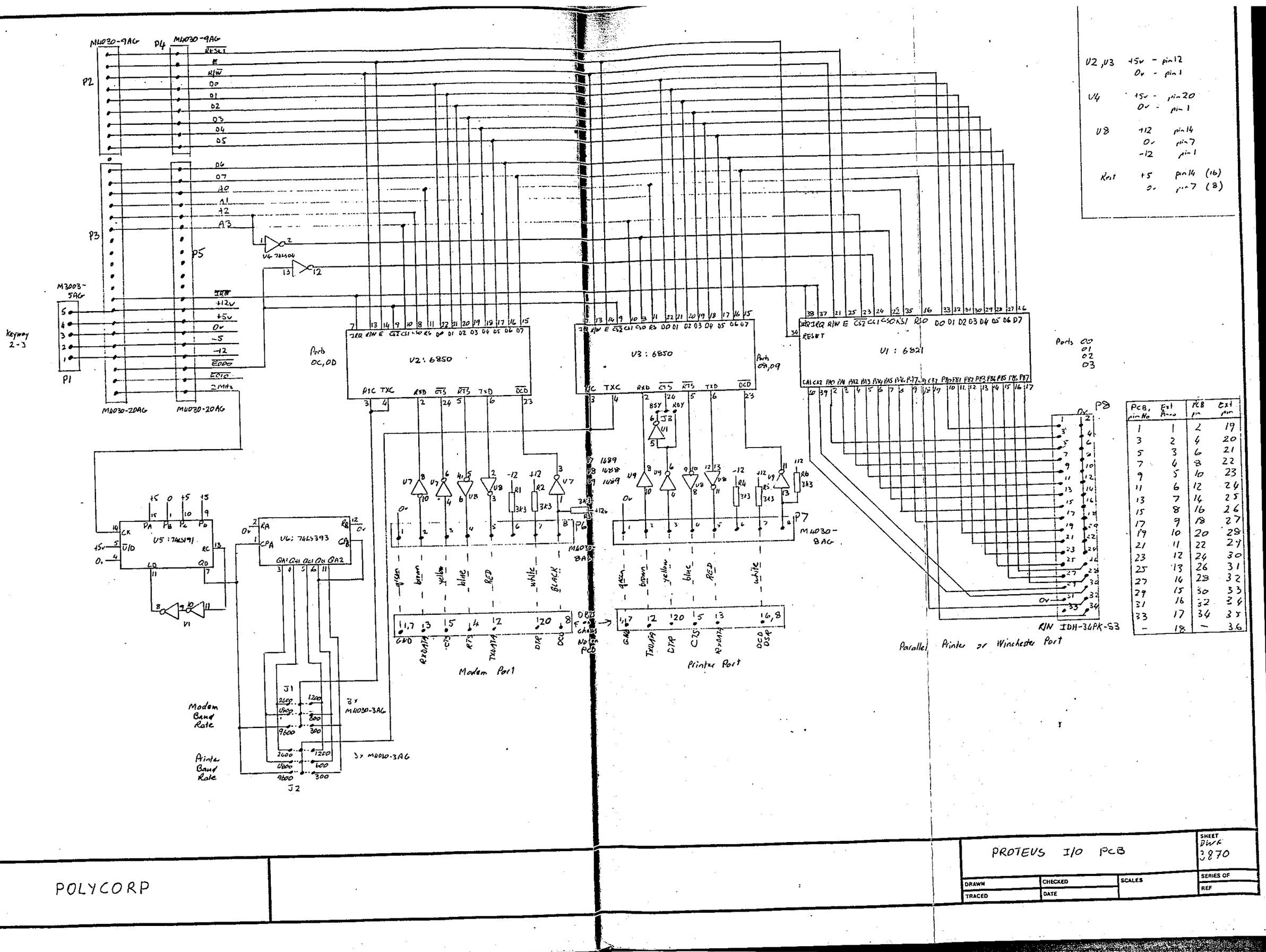
POLYCORP

Amendments
11/2/85. ILR co 3/83

POLY DISK CONTROLLER PCB, SINGLE DENSITY
Circuit Diagram / Component Location

DWG 200·0

DRAWN ILA | CHECKED | SCALES | SERIES OF
TRACED | DATE 11/11/71 | | REF



PCB pin No	Ext Conn	PCB pin	Ext pin
1	1	2	19
3	2	4	20
5	3	6	21
7	4	8	22
9	5	10	23
11	6	12	24
13	7	14	25
15	8	16	26
17	9	18	27
19	10	20	28
21	11	22	29
23	12	24	30
25	13	26	31
27	14	28	32
29	15	30	33
31	16	32	34
33	17	34	35
-	18	-	36

V2, V3 +5v - pin 12
0v - pin 1

V4 +5v - pin 20
0v - pin 1

V8 +12 pin 14
0v pin 7
-12 pin 1

Res +5 pin 14 (16)
0v pin 7 (8)

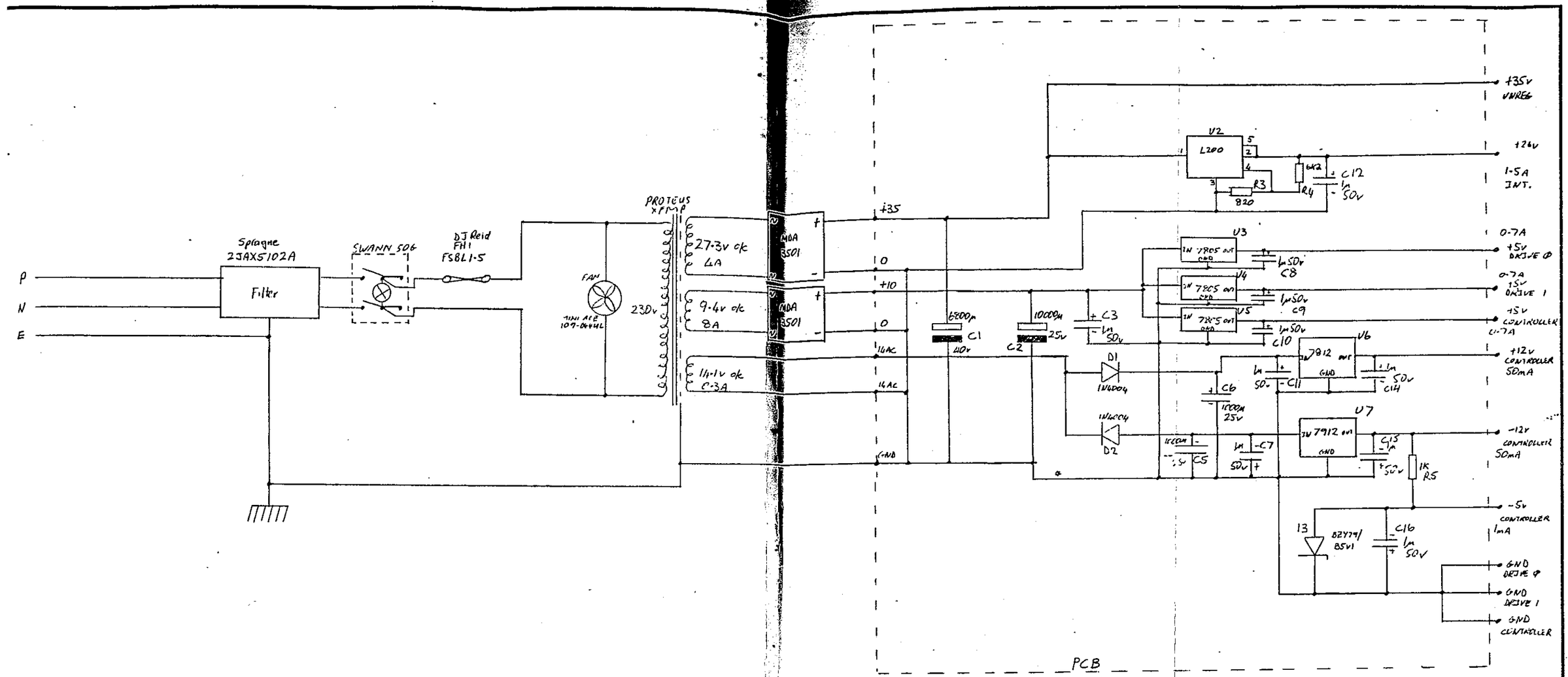
POLYCORP

PROTEUS I/O PCB

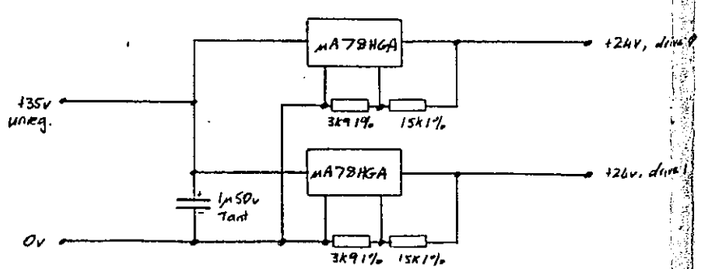
SHEET DWG 3870

DRAWN | CHECKED | SCALES | SERIES OF

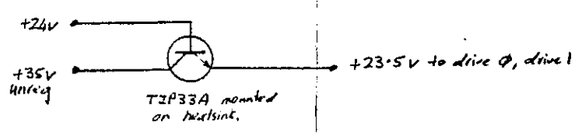
TRACED | DATE | REF



Rear Panel (Anst)

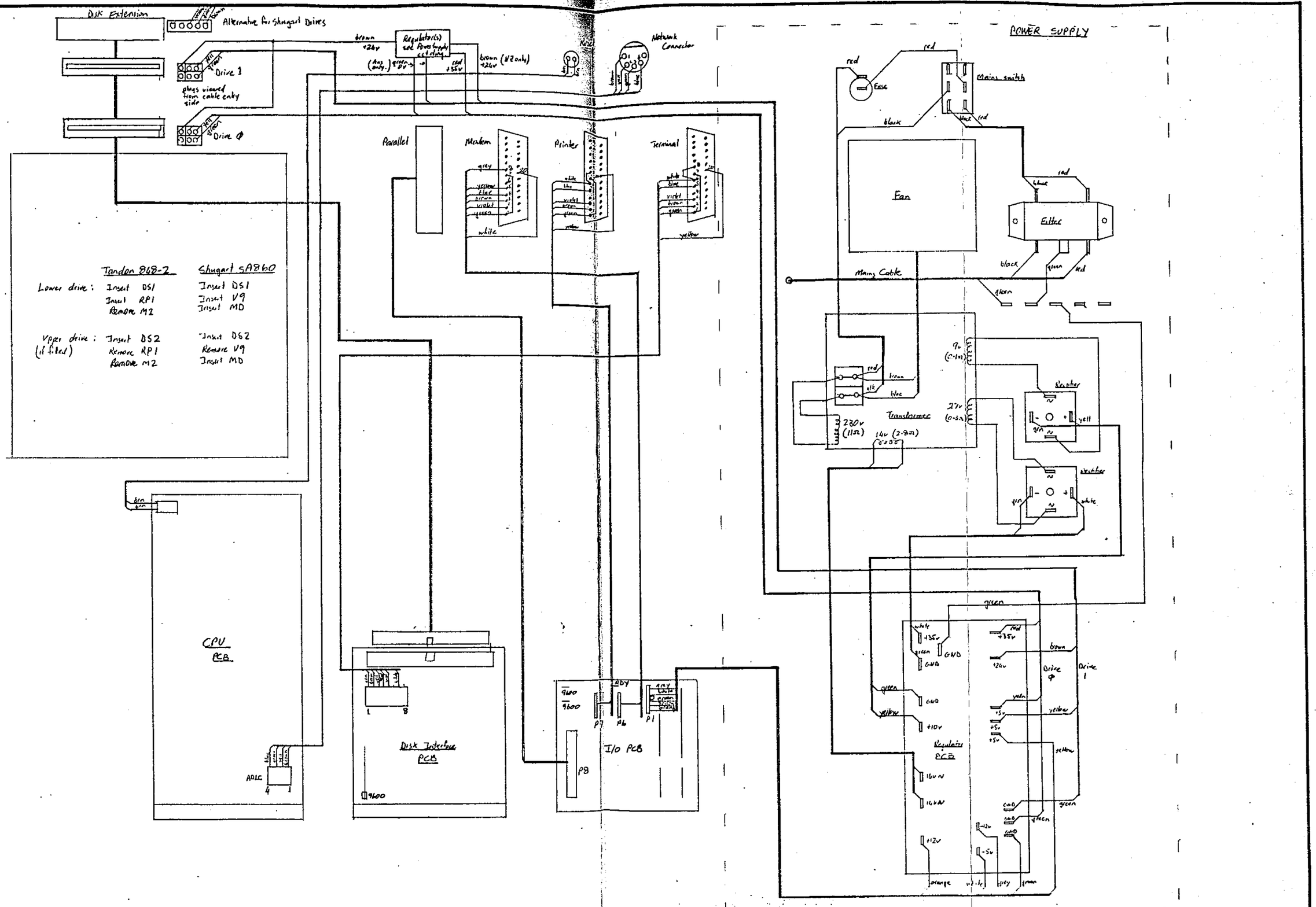


Rear Panel (NZ)



POLYCORP

B/2V3/84 WBM 11/2/85 ICR C.O. 10/83, 7/84 20/3/85 WBM CHANGE M/SWITCH REMOVE MCON	TWIN DISK UNIT (PROTEUS) Power Supply		SHEET DWG 2100·1
	DRAWN	CHECKED	SCALES
	TRACED	DATE	SERIES OF REF



POLYCORP

Amendments
12/1/85 JCR CO 10/83, 7/84
20/1/85 WBT REMOVE NEON

PROTEUS COMPUTER
Wiring Diagram.

DRAWN	CHECKED	SCALES	SHEET DW6 2038-1
TRACED	DATE		SERIES OF REF