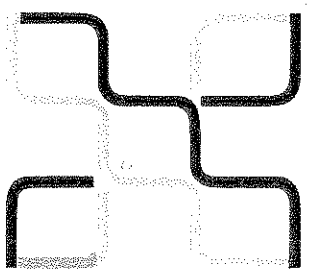
POLY-1 COMPUTER

Technical manual



POLY-1 COMPUTER

Technical manual

CONTENTS

1.0 General

This manual describes the hardware of the Poly-1 from a technical point of view. It is intended for use by hardware test and service technicians and for general reference. Related manuals which should be read in conjunction with this manual are -

POLY-1 FIELD SERVICE GUIDE

POLY EQUIPMENT ENGINEERING DESCRIPTION

POLY-1 SPECIFICATIONS

POLY SYSTEM SOFTWARE MANUAL

2.0 COMPUTER PCB

The computer PCB can be regarded as a micro-processor with external memory and input-output ports, together with circuitry to form a video signal from the contents of part of the memory. In fact this latter function accounts for a large part of the circuitry on the board.

NOTE In the descriptions which follow, many logic signals have names eg RAS. These names correspond with the names shown on the circuit diagram beside the connection OR to the name of a pin of an IC. If the signal is active in the low state it will be preceded by a - sign eg -RAS.

2.1 ADDRESS MAPPING

In order to address more than 64K of memory, software controlled address decoding is used which enables the logical address of physical memory blocks to be controlled. A separate scheme is used to protect the system memory and I/O ports from direct access by the user.

2.1.1 SYSTEM MODE OR UNPROTECTED MODE

In this mode addresses greater than $E000 are used to access the I/O ports, text screen, and system ROM. Addresses less than $E000 are decoded in the same manner as in the user or protected mode.

System mode is entered on Reset or by any Hardware or Software interupt. (U43.9 low).

The system address decoding shown in the following table is not software selectable.

SYSTEM AREA MEMORY MAP

ADDRESS	BUFFERS ENABLED	MEMORY/IO ENABLED	
E000-E003	U76, U67	U15	Video control PIA 6821
E004-E006	" "	Optional RS232 Interface	
E00C-E00F	" "	U16	Keyboard PIA 6821
E020-E027	" "	U18	Timer 6840
E030-E037	" "	U2	6854 Data Link Controller
E040	N/A		Set Protect Flip-Flop after 1 E cycle
E050-E05F	N/A	U84	Dynamic Address Translator. Contents define decoding of User Memory.
E060	N/A		Select Map 1 of Dynamic Address Trans.
E070	N/A		Select Map 2 of Dynamic Address Trans.
E800-EBBF	U76,U67,U40	U50,U51	Teletext 1 screen.
EBC0-EBFF	U76,U67,U40	U50,U51	System data.
EC00-EFBF	U76,U67,U39	U48,U49	Teletext 2 screen.
EFC0-EFFF	U76,U67,U39	U48,U49	System data.
F000-FFFF	None	U86	System Program ROM.

2.1.2 USER OR PROTECTED MODE (ALSO APPLIES TO SYSTEM MODE <$E000)

User mode is selected when U43.9 is high. This is set by software from system mode as follows:

```
STA $E040
RTI
```

Obviously, the software must ensure the required registers are on the stack.

In the user mode the selection of what physical memory resides at what address is controlled by the contents of the dynamic address translator U84. This IC is programmed from system mode. A SWI instruction must be used to program it from user mode.

For rapid switching of the decoding between two preset maps, a hardware selection between MAP1 and MAP2 is available. Once again it can only be changed while in the system mode or by a SWI instruction.

The following two maps are those set up by the Exorcisor Test program. The standard MAP1 is the same as below, except that the two blocks at $C000-DFFF and $E000-FFFF are reversed. The MAP2 given below is the standard MAP 2 selected on reset, however a different MAP 2 is sometimes used by BASIC.

MAP 1 (Exorcisor test program)

CPU Address A15,14,13	Hex	DAT Address	DAT Contents	Physical Address A16,15,14,13	Hex	Memory
000	0000	E050	0	0000	0000	RAMBANK1
001	2000	E051	1	0001	2000	RAMBANK1
010	4000	E052	3	0011	6000	RAMBANK2
011	6000	E053	8	1000	10000	RAMBANK4
100	8000	E054	4	0100	8000	RAMBANK3
101	A000	E055	6	0110	C000	BASIC1,2
110	C000	E056	7	0111	E000	BASIC3,4
111	E000	E057	5	0101	A000	RAMBANK3

MAP 2

CPU Address A15,14,13	Hex	DAT Address	DAT Contents	Physical Address A16,15,14,13	Hex	Memory
000	0000	E058	0	0000	0000	RAMBANK1
001	2000	E059	1	0001	2000	RAMBANK1
010	4000	E05A	3	0011	6000	RAMBANK2
011	6000	E05B	8	1000	10000	RAMBANK4
100	8000	E05C	4	0100	8000	RAMBANK3
101	A000	E05D	9	1001	12000	RAMBANK4
110	C000	E05E	5	0101	A000	RAMBANK3
111	E000	E05F	2	0010	4000	RAMBANK2

Notes:-

(1) The graphics 1 screen is located at a physical and logical address of 4000, ie a logical address of E000 only in MAP2.

The graphics 2 screen is located at a physical address of 8000 in both maps.

(2) When switching maps the program counter and stack pointer should be in an address which decodes the same before and after the switch.

BUFFERS AND IC'S ENABLED

	MEMORY IC'S ENABLED	BUFFERS ENABLED
RAMBANK 1	U97 - U104	U76, U87
RAMBANK 2	U111 - U119	U76, U87
RAMBANK 3	U126 - U133	U76, U88
RAMBANK 4	U140 - U147	U76, U88
BASIC ROMS	U89 - U92	U76, U88

2.2 SYSTEM ADDRESS DECODING

System mode is selected by a vector fetch (interrupt or reset) by the 6809. This is detected by U55 (pins 8-10) which reset both parts of U43 and immediately selects system mode. This means that the area above $E000 should never be used for the stack. User mode is selected by the CPU accessing address E040 U43 pin 9 will go high at the end of the access cycle and U43 pin 12 will go high at the end of the following cycle. This means the CPU can execute an RTI instruction before the address decoding changes.

The system address decoding is enabled whenever in the system or unprotected mode and when the address selected is > or = $E000.The system is unprotected when U43 pin 12 is low. This enables the pin 5 input to U63.

When the address selected is greater than $E000, U55 pin 6 will be low and enable the pin 4 input to U63. U63 and U54 then decode these addresses for all of the peripherals and memory in the system area. The decoding is not necessarily complete, ie some devices may appear at more than one address.

Both U63 and U54 are enabled only while E or Q is high, ie they are disabled during the first quarter of the microprocessor cycle while all the address lines are changing. This means there will not be glitches on the decoded outputs.

The address lines input to the system address decoder are not affected by the Dynamic Address Translator, ie decoding is fixed by the hardware.

2.3 DYNAMIC ADDRESS TRANSLATOR

This is used to control the mapping of physical memory into the address space of the 6809. It is programmed (from system mode) at a sequence of addresses from $E050 to $E05F. The lower 4 bits of the data bus only are relevant and must be the logical inverse of the outputs required. See the table in section 2.1.2 for the correspondence between the address to program and the logical addres affected.

U89 is the 4 bit by 16 word memory. When being programmed, its address lines come from the lower four address lines and its data input lines come from the lower four bits of the data bus. In its normal mode it is read only and its address line inputs come from the CPU high order address lines and its data outputs form the new high order address lines. Thus it creates a translation table between the CPU (logical) address lines and the physical address lines.

Also related to this is the MAP1/MAP2 flip-flop. The purpose of this is to rapidly switch between two predefined address maps. U53 (pins 8-13) forms the flip-flop. MAP1 is selected by accessing $E060 from system mode and MAP2 is selected by accessing $E070. The MAP1/MAP2 signal is used as an address input to the DAT RAM.

2.4 USER ADDRESS DECODING

The user address is decoded with respect to the outputs of the DAT (compare the system address which are decoded with respect to the CPU addresses). NOTE that a seventeenth address line (A16) is generated by the DAT and takes part in the decoding.

The physical address of the various parts of memory are shown in the table in 2.1.2.

U82 and associated gates decode the user addresses in 16K chunks for the four banks of dynamic RAM and in 4K chunks for the BASIC ROM'S.

The user addresses are enabled only when E is high, ie only during the second half of a CPU cycle.

The four BASIC Roms (U89-92) are enabled directly by their respective decoded address lines. At the same time U88 and U76 buffers are enabled.

2.5 DYNAMIC MEMORY

2.5.0 GENERAL

The dynamic memory IC's are operated on a 0.5 usec cycle, ie half the period of the CPU cycle. During the second half of a CPU cycle (E high) they are addressed by the CPU. During the first half of a CPU cycle they are addressed by the graphics hardware. There are two separate busses to the dynamic RAMs to enable the two independent graphics screens.

2.5.1 CPU ACCESS (E HIGH)

Only one row of RAMs (or none) will be enabled ie the row which is addressed. This row is enabled by -RAS pulsing low. -CAS always pulses low as it has no effect if -RAS is not present. During this time the R/W line comes from the CPU R/W line. The address lines come from the CPU address (via the Dynamic Address Translator).

2.5.2 GRAPHICS ACCESS (E low)

Rows 2 and 3 are enabled for read - ie -RAS pulses low, -CAS pulses low and the R/W line is always high. The address lines come from the pixel counter - U123 and U137. As the pixel counter cycles the row addresses at a much faster rate than the required 2msec, refresh is automaticaly performed.

Rows 1 and 4 are refreshed only on every 8th complete cycle of the lower 7 address lines, in order to conserve power. When they are refreshed only -RAS is pulsed low.

2.5.3 ADDRESS MULTIPLEXING

The row (lowest) 7 bits are first applied. Then -RAS goes low. Then the column (highest) 7 bits are applied and -CAS goes low. See the timing diagrams for details.

The above applies for both CPU and graphics addresses - the CPU address comes from the 6809 (with the higher two bits coming from the DAT output) and the grahics addresses coming from the pixel counter U123/U137.

The addresses are multiplexed at the appropriate times onto an intermediate bus by U95, U109, U124, and U138 and then applied to the RAMS via buffers U96 and U139.

2.6 GRAPHICS GENERATION

The pixel counter consisting of U123 is used to address the dynamic memory during the reading of the data for display. The pixel counter is reset during the vertical interval and incremented at the end of each byte read. (It is not incremented until the first byte has been read). Thus, the displayed bytes are addressed sequentially from the top left corner of the display to the bottom right. In fact only 8192 bytes are displayed - this gives 204 full rows plus a part row which is not intended to carry any data.

The data from the graphics memory is read out of the memory during the first half of the CPU cycle. Two parallel 8 bit bytes are read out, one for each graphics screen. The two bytes are latched for 0.5 usec in U77 and U78 in order to display the graphics more or less together with the text. The two high order bits of each byte are then latched for the next 1usec in U58. These bits define the colour for that period. Meanwhile the low six bits of each byte are latched into U69 and U70 and then shifted out with one bit being clocked out every 167nsec. These bits form the pixels for display, with the display colour being detired (for the whole six pixels on each screen) by the two high bits.

When the 480 mode is selected, the two groups of six bits are latched into U69 and U59, one bit then being clocked out every 83nsec. The GR1 video will contain the high resolution data and the GR2 video will not be used.

The pixel and colour informaton is combined and merged with the other screens as described in section 2.9.

2.7 TELETEXT MEMORY

The teletext memory consists of 4 only 1K x 4 static RAMS (U48 - U51) and is operated in a similar manner to the graphics memory, ie addressed by the CPU while E is high and addressed by the display hardware while E is low. There are two separate busses to the memory to enable the display of two independent text screens.

2.7.1 CPU ACCESS (E HIGH)

The address lines are obtained from the CPU address bus via multiplexors U44-U46. The read/write line is obtained from the CPU for the block of memory which is addressed (if any). For the block(s) of memory which are not addressed the read/write line is held high ie in the read mode. The appropriate data bus buffer (U39 or U40) is enabled for the block of memory addressed (if any).

NOTE If neither block of teletext is addressed by the CPU, the address lines remain switched to the display address.

2.7.2 TELETEXT ACCESS (E LOW)

The address lines are obtained from the display row/column information, via multiplexors U44-U46. In order to calculate the address from the information provided by the teletext timing generator (U42) U47 is used to count the columns with the rows being provided directly by U42. U35, U36 and U37 are then used to calculate the address as 40*ROW + COLUMN (plus the base address of the block).

The read/write line to the memories is held in the read state.

2.8 TELETEXT TEXT GENERATION

As described above, the memory is addressed during the time E is low by the current display position, starting from top left and working sequentially to the bottom right. Two 8 bit bytes are read from the memory every E cycle and latched by the two character generators U30 and U32. An exception is the most significant bit of each byte which is latched by U28 and then delayed for two and half cycles by U28 and U29. The two character generatrs each generate three serial outputs - R, G and B. These outputs are logically inverted if the most significant bit of the byte is a one in order to form inverse video. Note that a blanking signal is gated with the inverse video signal so that inverse video cannot occur outside the display area.

2.9 COMBINED VIDEO GENERATION

This section of the logic generates the RGB video signal output from the outputs of the character generators, and graphics generators. The graphics pixels are split into colours, although the text information is already coloured. This logic also provides the overlay or mix of the various screens and enables or disables the screens depending on the values programmed into the video control locations to be described later.

2.9.1 SCREEN OVERLAYING AND MIXING

In the punch-through (or overlay or priority) mode, the screens have a fixed priority order, ie the output of the circuit will consist of the colour defined by the highest priority screen which is enabled and is not black.

The priority is, highest to lowest:

1. Teletext 1
2. Graphics 1
3. Teletext 2
4. Graphics 2
5. Background

Note that if the 480-Graphics is enabled, it has the same priority as graphics 1 and graphics 2 is not used.

In the mix mode, Graphics 1, Teletext 2, and Graphics 2 have the same priority and their colours are mixed together by logically ORing the primary colours present on each screen.

This is achieved by, in fact, always logically ORing the various sources of each colour (with U10,U11 and U12) but when punch through occurs, the signals which are not required are disabled prior to U10, U11 and U12.

If Teletext 1 is non-black, indicated by U24 pin 3 being on, then the three colours of teletext 2 are disabled with U22b and U23a and b, Graphics 1 is disabled with U22a, Graphics 2 is disabled with U20, and then background is disabled with U21a.

If Graphics 1 is non black, indicated by a low level on U22 pin 6, then the background is disabled with U21a. If also, priority mode is selected, then U6 pin 6 will be a low level and Teletext 2 and Graphics 2 will be disabled with the same gates mentioned above.

If Teletext 2 is non black, indicated by a low level on U21 pin 8, then the background is disabled. If also, priority mode is selected, then U6 pin 8 will be a low level and Graphics 2 will be disabled.

2.9.2 GRAPHICS COLOUR

The graphics pixels are initially coloured by the higher two bits of each byte. These two bits are applied to U13 pins 2 and 3 (Graphics 1) and pins 14 and 13 (Graphics 2). If there is a pixel present, the screen is enabled and it is not punched out by a higher priority screen; the appropriate enable input of U13 is activated. This will activate one of the outputs of U13 which will then activate U10 (Red), U11 (Green), or U12 (Blue). These gates function as OR gates to mix the various signal sources for each colour.

The graphics pixels can also activate another primary colour when they are on (a constant colour over the whole screen). This colour is supplied by the video control PIA in binary form for each screen. The individual colours are generated by U8 in the same manner as U13.

2.9.3 BACKGROUND ADDITION AND VIDEO OUTPUTS

U7, R1-R17 and Q1 to Q3 are used to generate 75 ohm outputs, with a (terminated) output voltage of 0V (black level), +0.7V (white level) and approximately +0.3V (background).

2.10 INTERNAL PERIPHERALS

2.10.1 VIDEO CONTROL PIA

This PIA is used to enable the program to detire logic levels which are available to the video generation hardware to control various modes and functions.

The PIA is addressed in the system space at $E000 to $E004. The outputs are used as follows:-

PA0		not used. Connected to CA2.					
PA1	(	mix colour	0) Blue	1) Green	0) Red	1) No	
PA2	(	Graphics 1	0)	0)	1)	1) Mix	
PA3		1 = Enable Teletext 1 screen					
PA4		1 = 480 Graphics mode. 0=240 Graphics mode.					
PA5		1 = Enable Graphics 1 screen or 480 Graphics screen.					
PA6		1 = Mix Mode 0 = Priority mode					
PA7		Must be 0. Connected to PA7 and timer G3.					
PB0		1 = Enable Teletext 2 screen.					
PB1		1 = Enable Graphics 2 (must be 0 for 480 Graphics)					
PB2	(	Mix colour	0) Blue	1) Green	0) Red	1) No	
PB3	(	Graphics 2	0)	0)	1)	1) Mix	
PB4		1 = Enable Red Background					
PB5		1 = Enable Green Background					
PB6		1 = Enable Blue Background					
PB7		Not used.					
CA1		Connected to PA7 and timer G3. Must be 0.					
CA2		Not used. Connected to PA0.					
CB1		Not used.					
CB2		Not used.					

2.10.2 TIMER AND BEEPER

U18 is the timer. It is used to keep time of day and also to provide a variable frequency beeper. Apart from the beeper it has no external connections. It is addressed at $E020 - $E027 in the system address space.

The beeper is driven by the Q3 output.
C1 input is driven by Q2. This increments timer 1 when timer 2 resets.
Thus timer 3 is used for the beep, and timers 1 and 2 for time of day.

NOTE that the G3 input is driven by PA7 of the video control PIA. Therefore for the beeper to operate PA7 must be 0.

2.11 TIMING

2.11.1 CPU and TELETEXT TIMING GENERATION

All timing is initiated by the 12MHz crystal controlled oscillator. This is divided to form a 4MHz clock for the 6809 (U65) and a 6MHz clock for the teletext timing generator (U42). Both U65 and U42 divide their inputs to give a 1MHz clock. These can start up out of phase. This condition is detected by U68 pins 11-13 which stops the clock going to the teletext timing generator for the number of 12MHz cycles required to get the 6809 and the teletext timing generator in phase. This is defined to be when E and F1 are always complimentry. In fact because of varying propagation delays there will be short (<30nsec) instances when E and F1 are not exactly complimentry. This is filtered by R42 and C3.

The after hours sync output by the teletext character generator is used for the video to inhibit the interface generated by the character generator (and provide less flicker on text characters) the teletext timing generator is reset to line 0 whenever it reaches line 314. This gives a total number of lines of 314 per field instead of 312 1/2. To maintain exactly 50Hz vertical scan and reduced interaction with the mains, the 12MHz oscillator in fact is 12.0576.

Details of timing of the dynamic memory, graphics and video is shown in diagrams.

2.12 I/O PORTS

2.12.1 KEYBOARD

The keyboard is connected to a PIA at address $E00C - $E00F in the system address space.

The keyboard is connected to the PB0-PB7 lines, with the strobe connected to PB7 and CB1. This enables the strobe to generate an interupt as well as to be read at any time. The lowest significant data bit is connected to PB0 and the most significant data bit to PB6.

The CA2 output is also connected to the T/B input to the teletext timing generator, and the CB2 output is connected to the BCS input. These functions are not related to the keyboard but to the teletext large character mode.

PA0 - PA7 are not currently used.

2.12.2 DATA LINK

The MC6854 Advanced Data Link Controller is located in the system address space at location $E030 - $E037. Note that pairs of addresses are assigned to each register to enable two byte transfers to the same register with a double byte load/store instruction.

The data is transmitted at RS232 levels for best noise immunity. The following four lines run from each POLY towards the disk unit ("up loop") and towards the last POLY ("down loop").

Pin 1. Data from Disk Unit towards last POLY
Pin 2. Clock from Disk Unit to all POLYS
Pin 3. Ground
Pin 4. Data from last POLY towards Disk Unit

The data from the disk unit is connected to the RXDATA input to the 6854. The data to the next POLY is connected obtained from the TXDATA output of the 6854. During the time the disk unit is transmitting, the 6854 will transmit the same data as it receives.

The data going towards the disk unit can come from one of two sources, controlled by the -RTS output of the 6854. (This output has no relevance with regard to transmitting or not transmitting).

When -RTS low the data from the next POLY on the network is routed back to the previous POLY on the network (towards the Disk Unit).

With -RTS high the POLY routes its own transmitted data back towards the disk unit.

Normally the only POLY to route its own transmitted data back towards the disk unit is the last on the network.

However, during loops set up all POLYS loop their own transmitted data back. Then one by one they are commanded to loop back the data from the next POLY. During this time they are assigned addresses.

3.0 VIDEO MONITOR

This consists of a main PCB with four daughter PCB's, and a further small PCB on the picture tube base.

3.1 POWER SUPPLY

The large power supply components are mounted on the main PCB. However the control circuitry is on the PPCONTROL BOARD.

The main power supply consists of D200 and C232 which rectify and filter the mains directly to give approximately 320 volts DC. TR200 then chops this and applies it to the primary of L206. Various voltages are then obtained from the secondaries of L202. L205 shapes the waveform which is approximately flat in one direction with much larger peaks in the other direction.

To drive the above operation a small auxillary supply is used. This consists of L202, D201-203 and C237. This produces approximately 18V DC, which is used to power the PP control PCB. This PCB drives the base of TR200 through L204 to provide the chopping of the main power supply.

Most of the video circuitry is isolated from the mains by L206, L204, L203 and L202. Components on the primary side of these transformers are directly or indirectly connected to the mains. Note that C232 stays charged for some time after the power is switched off, as indicated by the neon indicator glowing. Also note that many of the secondary voltages of L206 are also dangerous.

The PP control circuitry consists mainly of U100 (TDA 2582). This senses the 148V DC output of L206 divided by R106, R102 and the mark/space ratio of the chopped waveform applied to the primary of L206 is controlled in order to regulate the 148V DC supply. R103 can be adjusted to set the 148V DC output. Overvoltage protection is built in, as is overcurrent protection via the current sense transformer L203. If there is an overload the supply will switch off and on a number of times before finally switching off completely. The EHT voltage (~27KV) is obtained from L206. This is divided to give the focus voltage. Finally the G2 voltage is obtained by rectifying the horizontal deflection voltage to be described later.

The chopping frequency is normally locked to the input horizontal syncs, ie 15625Hz. In the absence of input syncs, the frequency will be slightly lower.

3.2 VIDEO RGB CIRCUITRY

Most of this circuitry is on the RGB Board.

The R, G & B inputs (0.7 v p-p) are applied to the teletext input of U1, TDA 3501. The normal video inputs to U1 are not used. The outputs of U1 are amplified with T1 and T2 (blue), T3 and T4 (green), T5 and T6 (red). A portion of the output signals are used as feedback to U1. A small DC signal can be added to the feedback voltage to provide a DC shift of the outputs. This is adjustable with R6, R11 and R16 which are used to balance the black level of the three guns. The green and blue gains are respectively controlled by R36 and R37. These can be adjusted to balance the white level of the three guns. R216 and R217 are used to adjust the contrast and brightness respectively. An external switch is also connected to the contrast control, to provide two levels of contrast.

3.3 SYNC GENERATON

Most of this circuitry is on the SYNC Board.

U 50 and associated componentry provides a phase locked oscillator locked to the sync input which generates the horizontal sync pulses to synchronise the power supply and provide horizontal deflection. The vertical sync output is obtained by integrating the sync input for non-standard signals or by dividing down the horizontal sync for standard signals. As our sync signal is not quite standard (ie, 628 lines per frame instead of 625), it is presumed that the former condition applies.

R72 provides a DC adjustment to the VCO feedback signal, thereby providing a small phase adjustment to the output. This can be used to centre the picture.

R215 is the horizontal frequency control. This should be adjusted with the 2 pin plug on the sync PCB shorted to obtain a picture which is almost locked. The picture should lock up solidly when the short is removed.

R55 is for adjusting the sync level input to U50 and should be adjusted to the centre of the range over which the picture is stable.

NOTE

In the absence of sync pulses generated by U50, U1 will switch off its RGB outputs in order to confuse technicians. Also the power supply will operate at a lower frequency.

3.4 HORIZONTAL DEFLECTION

Most of this circuitry is on the main board, except for the E-W correction and width control on the E-W board. The horizontal deflection yoke is driven by the 148 volt output of the power supply - switched by TR201 and shaped by L208 and C219. The base of TR201 is driven by a winding on L206. The deflection voltage (1200 v pk) is rectified by D216 and used to generate the G2 voltage for the picture tube. Thus if the horizontal deflection is not operating the picture tube will be cut off.

NOTE: A fault in the horizontal deflection circuitry, eg short in L208 or TR 201 can overload the power supply sufficiently for it to switch off. If the overload is removed by un-plugging PL207 with its associated link it is likely that there is a fault in one of the above components.

The horizontal deflection voltage is adjusted slightly during the vertical scan by the E-W board, to minimise "pin-cushion" distortion.

3.5 VERTICAL DEFLECTION

All of this circuitry is on the main board.

U200 and associated circuitry consist of a synchronised oscillator with amplification and output stages. R203 is used to ajust the oscillator frequency to the centre of the range which locks steadily, R206 is used to adjust the linearity, and R212 is used to adust the vertical deflection amplitude, ie height of the picture .

NOTE: If the vertical deflection fails, turn the unit off immediately.

4.0 KEYBOARD

The keyboard circuitry consists of the keyswitches connected in a row/column matrix, and an encoder IC which scans the switches and generates the appropriate ASCII code for any depressed switch.

The keyboard encoder outputs a (positive going) pulse on each of pins 39-32 in turn, and during each pulse, monitors the input pins 21-31. If the positive voltage reaches any of the input pins, the IC stops scanning and outputs the ASCII code corresponding to the depressed key from the row and column information. The strobe output is then set high.

Note that the SHIFT key is connected to an input of the IC and alters the generated ASCII code if it is pressed. If a control key is connected it functions in a similar manner. The CAPS-LOCK key however is used to alter bit 5 of the output code when the key is pressed, by selecting between 1 of 2 outputs from the encoder.

Most of the keys generate the required codes directly. However some of the unused ASCII codes are used for the special function keys. The circuit diagram shows the actual ASCII code generated by each key (alone, with shift key, and with control key), together with the keytop legend.

5.0 POWER SUPPLY

The power supply assembly consists of a mains filter, switch, fuse, neon and connector to the video module, and also a regulator assembly to generate the power for the computer logic board from the power supply on the video module. Various connectors and controls are also included.

5.1 REGULATOR ASSEMBLY

This produces the following voltages:-

+12V	at	30mA
+ 5V	at	2.5A
- 5V	at	1 mA
-12V	at	30mA

The input power to the regulator is extracted from extra windings on L206 on the video board. The two windings produce:

(1) Positive 8V pulses with large negative pulses, and
(2) Negative 12V pulses with large positive pulses.

The first of the above is rectified by D1 and filtered by C1. It is then regulated by U2 and T1 to produce +5volts. Note that the power for the regulator comes from the +12 volt supply mentioned below.

The second of the above waveforms is rectified by D2 and filtered by C2. This gives -12 volts for the computer board. The -12 volts is then regulated by R4 and D3 to give -5 volts.

+18V DC is also extracted from the video module ad regulated by U1 to give +12V DC.

NOTE that the power supply on the video module starts slowly, therefore the above voltages also start up slowly.

NOTE serial numbers up to 1099 used a different power supply.

6. OPTIONAL RS232C INTERFACE

This plugs into P9, P10 on the computer PCB. The ACIA, U1 is located at system address $E004 - $E005. The baud rate control register is at address $E006. The baud rates are as follows:-

00	:	9600
02	:	4800
04	:	2400
06	:	1200
08	:	600
0A	:	300

U5 is the write only baud rate register. Its outputs control data selector U6 to select the 16 times baud rate clock which is generated by U7 (16 x 9600) and U8 (16 x other rates).

NOTE that the cable from the PCB to the DB25 connector can be wired in either of two ways, to configure the interface as either a modem, or a terminal. This is shown on the circuit diagram.

7.0 OPTIONAL VIDEO INTERFACE

This interface is installed as a looping connection between the computer PCB video output and the Video Monitor input. It generates both PAL video for connection to a monnitor and RF for connection to a TV receiver. It obtains its power from a looping connection between the power supply and the computer PCB.

U1, U2, and U3 digitise the incoming video from its "analogue" levels into TTL levels. When the video is black (0V) both outputs of each IC will be a TTL low. Whem the inncoming video is half intensity (0.3V) the LOW output will be a TTL high, and when the incoming video is full intensity both outputs will be TTL high levels.

Q1 and Q2 generate TTL sync pulses from the incoming sync signal. U4 generates a burst enable pulse for the correct duration of the colour burst output and U5 generates a half line frequency square wave.

All these TTL signals are applied to U6 which generates luminance and colour difference signals (Y, B-Y, R-Y). These signals are applied to U7 which contains the subcarrier and RF oscillators and modulators. The B-Y and R-Y signals are used to modulate two 90 degree offset components of the 4.43MHz signal and then these two signals and the luminance Y are summed at pin 13. This point is used to drive the video output via emitter follower Q3 and also to modulate the RF carrier. The RF frequency can be adjusted in the range 50-70 MHz (ie for the lowest channel of Australian and New Zealand TV) by altering the spacing of L1, and the subcarrier frequency can be adjusted with CV1.

8.0 TEST PROCEDURE

8.1 COMPUTER PCB

The computer PCB should first be tested on the EXORCISOR using the program POLYxx (xx refers to the version number). This will test most of the functions of the PCB and also provides diagnostics as shown in the menu. The complete test of the PCB will occur in the final test of the POLY.

8.2 Video

The small PCBs should be tested on a known working system.

The large PCB should be tested as follows -

(1) Install all small PCBs, picture tube,cables etc except PL207.
Connect mains and switch on.
Check for 330v DC accross C232.

(2) Check for +18V on input of U201 (7812) and +12V on output

(3) Check for +148V on cathode of D210.
If present switching power supply is working.
If not check TR200 and associated components.

(4) Check for +33V on cathode of D211
+18V on cathode of D212
+225V on cathode of D213

(5) Switch off mains.
Connect PL207 and some video input signal.
Switch mains back on and check for picture.
If not present try adjusting brightness and G2 voltage.
If gray raster now present problem must be lack of video signal or lack of sync which switches off video!
If no gray raster present check for +675 volts on top end of R91 on Picture Tube Base Board. (This is obtained by rectifying horizontal deflection voltage).
If not present check Tr201, L208 etc.

(6) If no vertical deflection switch off immediately. Check U200 and associated components.

(7) The video should be adjusted as described in the FIELD SERVICE GUIDE.

Note The power supply is protected against overcurrent. If it overloads it switches off and on again for up to about 10 times before it stays off until the power is switched off and back on.

8.3 POWER SUPPLY

A complete video system OR a video board with PP Control and Sync daughter boards is required.
Connect mains lead to Video board (PL 210).
Connect transformer extra windings to power supply board.
Connect PL213 to power supply board +18V.
Connect output of Power supply to Dummy Load.
Switch dummy load on.
Switch power supply on.

Check the terminals on the dummy load.
+12 V must be 11.0 V to 13.0 V
+5 V must be 4.75 V to 5.25 V
-5 V must be -4.5 V to - 5.5 V
-12 V must be -10 V to -13 V

To check the network cable, plug the Molex plug onto the dummy load. Plug the free end of the cable into the socket on the power supply chassis.
Check that all three LEDs light up.

8.4 Final Test

The complete Poly should be connected to a Poly Disk Unit or Proteus computer and the program POLYTEST run.

When a network of POLYs is being tested, it should be checked that the last POLY on the network is capable of operating correctly when it is not the last one.

Item	Circuit Reference	PART	Qty	Each	Total
1	Cabinet	To Polycorp specs	1		
2	Chassis	" " " dwg 1600	1	✓	
3	Tube mtg bars	" " " dwg 1602	2	✓	
4	"POLY-1" Moulding Label	G Luhman.	1		
5	Keyboard cover plate	" " " dwg 1611	1	✓	
6					
7	Power Supply assembly	See separate list	1		
8	Keyboard assembly	" " "	1		
9					
10	Computer PCB complete	(Delphi) See separate list	1		
11	VDU Main PCB complete	" " " "	1		
12	RGB PCB complete	" " " "	1		
13	FP control PCB complete	" " " "	1		
14	Sync PCB complete	" " " "	1		
15	E-W PCB complete	" " " "	1		
16	Pict. Tube Base PCB complete	" " " "	1		
17	PCB holding extrusions	'Short' extrusions	5		
18	" " "	Long extrusions	2		
19					
20	Rubber for screen cut-out	Liter GZ1	1.5m	✓	
21	Rubber feet	DJ Reid HW102	4		
22	Rubber grommets for mtg chassis	PARA RUBBER #2	4		
23	Plastic screw covers		2		
25	Bases for above		2		
26					
27	Screen surround	To Polycorp specs.	1.		
28					
29	Set of cables.	See separate list	1		
30					
31	Pict. Tube assbly A37-570X-AT1200	Philips 9323 999 80007	1		
32	Degaussing Coil 14 inch	Philips 3122 138 75180	1		
33	EHT lead	Philips 4323 999 00012	1		
34					

POLYCORP

Date 5-5-82

Parts List for POLY-1 COMPUTER

Sheet 1 of 2

Item	Circuit Reference	Part	Qty	Each	Total
1	Grommets for tube mtg	~~AARA~~ RUBBER No. 5	4		
2					
3	Clip for EHT lead earth	?	1		
4					
5	Spring for agneding lead	Gerraid Springs.	1		
6	FASTON terminal " "	AMP 735 278	1		
7	Cable tie for degaussing coil	250mm cable tie	1		
8					
9					
10					
11					
12					
13					
14					
15					
16					
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34					

POLYCORP

Date 5-5-82

Parts List for

POLY-1 COMPUTER

				Each	Total
	KEYBOARD CABLE	Beware of equivalents. Pin 1 of IC must go to pin 1 of cable.			
	DIL plug ECS	Blue Moon → 609 - M161H	1		
	16way plug OR Robinson Nugent IDS-16PK	" " 609 - 1630	1		
	Cable	" " 171 - 16	1m		
	VIDEO - COMPUTER CABLE				
	5 way keyed 1-2 housing	M3011 - 5A	1		✓
	6 way no key housing	M3001 - 6	1		✓
	Terminals	M2578 - GL	10		✓
		NOW PART OF VIDEO			
	PICTURE TUBE BASE LEAD				
	7 way no key	M3001 - 7	2		✓
	Terminals	M2578 - GL	14		✓
	CONNECTIONS TO TUBE, DEGAUSING COIL				
	2way housing (V scan, degaussing)	M3001 - 2	2		✓
	4way housing (H scan)	M3001 - 4	1		✓
	Terminals	M2578 - GL	8		✓
	Wire 0.65 mm²	DJ Reid WIL03xx Total	20m		
	Focus lead	B&W EHT lead	0.7m		
	Termination	Philips 3122 131 61416	1		
	Speaker	Delphi 2½" 3252	1		
	Housing for speaker cable	M6471 - 02	1		
	Terminals for above	M2759 - GL	2		
	KEYBOARD EARTH LEAD				
	Faston terminal	AMP 735 278	1		
	M4 terminal	AMP 31890	1		

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Parts List for
Poly-1 Cables etc

Sheet 1 of 1

		Part	Qty	Each	Total
1	Chassis incl. heatsink	Dwg no.	1		✓
2	Mains Plug	PDL 40	1		✓
3	Mains cable	Alcal TPS flex 0.75 mm² 3 core	3 m		✓
4	Mains filter	SCHAFFNER FN 610-3/06	1		✓
5	Mains switch	DJ Reid SW28	1		✓
6	Fuse holder	DJ Reid FH1	1		✓
7	Fuse	DJ Reid FSBL1-5	1		✓
8	Neon	DJ Reid N6YL	1		✓
9	Clip for neon	DJ Reid N4	1		✓
10	Washer " "	DJ Reid N6	1		✓
11	Earth lugs	Utilux 1944	4		✓
12	Reset switch	DJ Reid SW16	1		✓
13	Contrast switch	DJ Reid SW51	1		✓
14					
15	Network cable	OR AWA 4D DJ Reid WIG25	4 m		✓
16	Network Plug	Newtrick NCSMC	1		✓
17	Network Skt	Newtrick NC5FP	1		✓
18	Network Cable anchor	DJ Reid HW122 type B?	1		✓
19	Mains Cable anchor	DJ Reid HW121 type A	1		✓
20					
21	Label	McKenzie & Holland	1		✓
22	Serial No.	NZ Labels	1		✓
23					
25	Housing for +18v cable	M3001-2	1		✓
26	Housing for contrast cable	M3001-4	1		✓
27	Housing for LOPT winding cable	M3011-4A	1		✓
28	Housing for mains cable term.	M3001-5	1		✓
29	Housing for PSU d/p cable	M3011-5B	1		✓
30	Terminals for above	M2578-GL	20		✓
31					
32	Faston connectors	AMP 735278	19		✓
33					
34					

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Parts List for

Poly-1 PSV MK 2

Sheet 1 of 2

			Qty	Each	Total
1	Housing for User Port, Reset	M 6471-03	2		✓
2	Housing for Network cable	M 6471-08	1		✓
3	Terminals for above	M 2759-GL	13		✓
4	TO220 Bush	Philips 9390 278 00112	4		✓
5	TO220 Washer	Philips 9390. 276 50112	4		✓
6	Miscellaneous wire 0.65 mm²	DJ Retd WIL03xx Total	20m		✓
7					
8	Cable ties	130mm cable ties	20		✓
9					
10	PCB	Polycorp # 820810	1		✓
11	4 way water	M3003-4AG	1		✓
12	Faston PCB tabs	Z836	8		✓
13	V1	7812 Philips 9323 999 50021	1		✓
14	V2	L200 " 9323 999 50057	1		✓
15	T1	60T93 " 9334 519 10112	1		✓
16	D1	BYW29 " 9333 912 80112	1		✓
17	D2	BYV95B " 9335 001 70113	1		✓
18	D3	BZY79/B5V1 9331 668 10112	1		✓
19					
20	R1	4E7 CR25 2322 211 13478	1		✓
21	R2	47Ω CR25 " " 13479	1		✓
22	R3	220Ω CR25 " " 13221	1		✓
23	R4	1K CR25 " " 13102	1		✓
25	R5	680 MR25 " 151 56801	1		✓
26	R6	820 MR25 " " 58201	1		✓
27					
28	C1	4700m 16v 2222 050 55472	1		✓
29	C2, C3	220m 16v " 034 65221	2		✓
30	C4	22m 16v " " 65229	1		✓
31	C5, C6, C7	2m2 25v " 122 56228	3		✓
32	C8	1n5 " 630 06152	1		✓
33					
34	Resistor for ~~Rbias~~ contrast sw.	4K7 CR25, 2322 211 13472	1		✓

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Parts List for

Poly-1 PSU Mk 2

Sheet 2 of 2

	Circuit Reference	Part No.	Qty	Cost Each	Cost Total
	U3, U24, U25, U38, U53, U80, U81, U83, U105, U110, U125, U135	SN 74LS00	12		
	U120	SN 74LS02	1		
	U56, U119	SN 74LS04	2		
	U7	SN 74LS05	1		
	U55	SN 74LS10	1		
	U9	SN 74LS11	1		
	U22, U23, U57, U79	SN 74LS20	4		
	U21, U62	SN 74LS21	2		
	U10, U11, U12, U120	SN 74LS30	4		
0	U6, U26, U27, U74, U106, U122	SN 74LS32	6		
1	U03, U73, U94, U134	SN74LS73	4		
	U31, U33, U68	SN74LS86	3		
3	U84	SN 7489	1		
4	U54, U63	SN 74LS138	2		
5	U8, U13, U82	SN 74LS139	3		
6	U44, U45, U46, U85	SN 74LS157	4		
7	U59, U69, U70	SN 74LS165	3		
8	U28, U29, U58, U107	SN74LS175	4		
9	U64, U66, U75, U95, U96, U109, U124, U139, U138	SN74LS244	9		
0	U39, U40, U67, U76, U87, U88	SN74LS245	6		
1	U35, U36, U37	SN74LS283	3		
	U77, U78	SN74LS373	2		
3	U47, U123, U137	SN74LS393	3		
5					
6					
7					
8	U4	MC1488	1		
9	U5	MC1489	1		
0	U48 - U51	2114 (250nsec)	4		
1	U86, U89, U90, U91, U92	2532	5		
2	U52	MC14022	1		
3	U41	MC14050	1		
4					

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Parts List for

Poly-1 computer PCB

Sheet 1 of 3

Item	Circuit Reference	PART	Qty	Each	Total
1	V97-104, V111-118, V126-133, V140-147	MCM4116 (200nsec)	32		
2	V42	SAA5020 (PROFESSIONAL ELEC)	1		
3	V30, V32	SAA5050 "	2		
4					
5					
6					
7	V65	MC6809	1		
8	V15, V16	MC6821	2		
9	V18	MC6840	1		
10	V2	MC6854	1		
11					
12	(V4, V5)	14pin DIL skt	2		
13	(V84, V97-104, V111-118, V126-133, V140-147)	16pin DIL skt	33		
14	(V48-V51)	18pin DIL skt	4		
15	(V39, V40, V67, V76, V87, V88)	20pin DIL skt	6		
16	(V42, V86, V89-V92)	24pin DIL skt	6		
17	(V2, V18, V30, V32)	28pin DIL skt	4		
18	(V15, V16)	40pin DIL skt	2		
19					
20	P4	16pin DIL skt IC-316-SGT heavy duty	1		
21	(V65)	40pin DIL skt IC-640-SGT heavy duty	1		
22	P9A	M4030-20AG	1		
23	P6, P10	M3003-5AG	2		
25	Beep, P11	M4030-2AG	2		
26	reset	M4030-3AG	1		
27	P5	M4030-8AG	1		
28	P9B	M4030-9AG	1		
29	D4	IN4148	1		
30	D1	IN4003	1		
31					
32	Q1, Q2, Q3	BC557 or similar	3		
33	Q4, ~~Q5~~, Q6	BC547 or similar	2		
34					

POLYCORP

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Parts List for

Sheet 2 of 3

				Each	Total
1	C3, C4, C5	100pF 63v	3		
2	C2	22µ/16v	1		
3	Decoupling C's	.1µF 63v Seimens	100		
4					
5	R53-R64, R69-R76	33Ω CR25	20		
6	R40, R45, R65-R68	47Ω CR25	6		
7	R3, R6, R9, R10	82Ω CR25	4		
8	R2, R5, R8	100Ω CR25	3		
9					
10	R42	220Ω CR25	1		
11	R1, R4, R7, R12, R13, R14	470Ω CR25	6		
12	R11, R15, R16, R17, R44, R46-R51	1KΩ CR25	11		
13	R24-R38, R41, R43, R52, R77	3K3Ω CR25	19		
14	R39	47K CR25	1		
15					
16					
17	PCB	# 820811	1		
18					
19	Relay	ITT A2810-12V	1		
20	Crystal	12.0576 MHz Series HC18-U	1		
21					
22					
23					
25					
26					
27					
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32					
33					
34					

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Parts List for

Sheet 3 of 3

Item	Circuit Reference	PART	Qty	Price Each	Price Total
1	U1	MC 6850	1		
2	U2	MC 1488	1		
3	U3	74LS27	1		
4	U4	74LS10	1		
5	U5	74LS175	1		
6	U6	74LS251	1		
7	U7	74LS191	1		
8	U8	74LS393	1		
9	U9	MC 1489			
10					
11	P1	M 4455-10AG	1		
12	P2	M 4455-20AG	1		
13	Polarising Pin	M 4161-1	1		
14	P3	M 4030-8AG	1		
15					
16	R1	3k3 CR25	1		
17					
18	Stand-offs		2		
19	Screws for above		2		
20					
21	DB25 connector	D Reid CS25S	1		
22	Housing	M 6671-8A	1		
23	Pins for above 0.1" terminals.	M 2759-GL	8		
25					
26	PCB	Progeni	1		
27					
28					
29					
30					
31					
32					
33					
34					

POLYSORB

Date		

Parts List for

ASSEMBLY OF POLY 1

VIDEO MONITOR

EAST/WEST BOARD 811101

Part #	Resistors	Qty
R87	2322 211 13152 1K5 CR25	1
R86	2322 211 13332 3K3 CR25	1
R85	2322 211 13682 6K8 "	1
R88	2322 211 13123 12K "	1
R89	2322 212 13123 12K CR37	1
R80	2322 212 13154 150K CR37	1
R84	2322 211 13274 270K CR25	1
R83	2322 211 12225 2M2 "	1
R82	2322 410 05059 47K Preset Vertical	1
R81	2322 410 05062 220K Preset Vertical	1
	Capacitors	
C81	2222 630 06332 3N3 100V Plate Ceramic	1
C80	2222 034 58109 10uF 63V Electro PCB	1
TR 80	9332 055 50112 BC 560 Transistor	1
TR 81	BF871 or BF 858	1
SKT 3	M3002-6A Socket	1
PCB	811101 Polycorp	1

SYNC BOARD 811102

R 64	2322 211 13109 10E CR25	1
R60	2322 211 13829 82E CR25	1
R58,65,61	2322 211 13102 1K CR25	3
R71	2322 211 13152 1K5 CR25	1
R69	2322 211 13222 2K2 CR25	1
R57	2322 211 13392 3K9 CR25	1
R59	2322 211 13472 4K7 CR25	1
R70	2322 211 13682 6K8 CR25	1
R63,54	2322 211 13103 10K CR25	2
R66	2322 151 41603 16K MR25	1
R68	2322 211 13333 33K CR25	1
R56	2322 211 13223 22K CR25	1
R62	2322 211 13274 270K CR25	1
R72	2322 410 03354 1K Preset Horiz	1
R55	2322 410 05057 10K Preset Vertical	1
C63	2222 122 55109 10uF 16v (SOLID ALUMINIUM)	1
C61	2222 424 42702 2N7 63V	1
C65	2222 352 58103 10NF 400V	1
C64	2222 629 06223 22NF 63V	1
C56, 60	2222 352 47104 100NF 250V	2
C53	2222 642 34151 150PF 100V	1
C58, 54	2222 034 59108n 1uF 100V	2
C57,~~63~~,52	2222 034 55109 10uF 16V	~~3~~ 2
C55, 51, 62, 59	2222 034 65229 22uF 16V	4
U50	9335 306 40112 TDA2576A	1
(U50)	M3406-16 IC Socket 16 Pin	1
SKT4	M3002-9A Socket 9Way	1
Plug	M3003-2A Plug 2 Way	1
PCB	811102 Polycorp	1
Links	'0' Ohm resistor ¼Watt	1

PP CONTROL BOARD 811103

R122	2322 212 13109 10E CR37	1
R127	2322 211 13479 47E CR35	1
R123	2322 211 13331 330E CR25	1
R121	2322 212 13102 1K CR37	1
R117,120,109	2322 211 13222 2K2 CR25	3
R104	2322 211 13272 2K7 CR25	1
R118,126	2322 211 13332 3K3 CR25	2
R119	2322 211 13392 3K9 CR25	1
R115,108	2322 211 13562 5K6 CR25	2
R100, R102	2322 151 56202 6K2 MR25	2
R110	2322 211 13103 10K CR25	1
R113,124	2322 211 13273 27K CR25	2
R128	2322 211 13223 22K CR25	1
R105	2322 211 13393 39K CR25	1
R114	2322 211 13563 56K CR25	1
R116	2322 151 54123 41K2 MR25	1
R125	2322 211 13154 150K CR25	1
R106	2322 151 41504 150K MR25	1
R111	2322 211 13274 270K CR25	1
R101,112	2322 211 1225 2M2 CR25	2
R103	2322 410 05054 1K Preset Vertical	1

PP CONTROL BOARD

C106	2222 630 06471 470PF 100V	1
C108, 103	2222 630 06102 1NF 100V	2
C107	2222 424 42702 2N7 63V	1
C111	2222 630 06472 4N7 100V	1
C105	2222 352 47223 22NF 250V	1
C102	2222 352 48683 68NF 250V	1
C104	2222 034 59108 1µF 100V	1
C110,101	2222 034 57478 4u7 40V	2
C109,100	2222 034 54479 47uF 10V	2
TR100	9332 435 90112 BC550B or BC550C	1
TR101	9332 219 40112 BC639	1
D100,107,103 104, 105, 106	9331 012 20112 BAW62	6
D108, 109	9331 892 10112 BAV21	2
D102	9331 178 10112 BZX79C12	1
D101	9331 177 40112 BZX79C6V2	1
U100	9334 783 90112 TDA 2582	1
LINK	'0' ohm RESISTOR	1
(U100)	M3406 - 16 SOCKET 16PIN	1
SKT5	M3002 - 12A SOCKET 12WAY	1
PCB	811103 POLYCORP	

R.G.B. BOARD

R1,2,3,4	2322 211 13829 82E CR25	4
R8,12,18,22,25, 27,32,35, 30	2322 211 13561 560E CR25	9
R21,26,31	2322 212 13821 820E CR37	3
R5	2322 211 13102 1K CR25	1
R10,15,20	2322 211 13122 1K2 CR25	3
R9,14,19	2322 211 13182 1K8 CR25	3
R7,12,17	2322 211 13893 39K CR25	3
R44	2322 211 13103 10K CR25	1
R41	2322 211 13153 15K CR25	1
R43	2322 211 13223 22K CR25	1
R23,28,33	2322 192 31803 18K PR52	3
R40,42	2322 211 13154 150K CR25	2
R24,29,34	2322 212 13683 68K CR37	3
R38,R39	2322 211 13823 82K CR25	2
R6,11	2322 410 05057 10K Preset Vertical	2
R16,36,37	2322 410 03357 10K Preset Horiz.	3
C11,12,13	2222 642 34159 15PF 100V	3
C15	2222 352 65103 10NF 400V (630V)	1
C4,5,6, 8,9,10,16, 17	2222 352 47223 22NF 250V	8
C1,2,3,	2222 352 48473 47NF 250V	3
C14	2222 031 65228 2m2 350V	1
C7	2222 22mF 40V	
T1,2,3,4, 5,6,	BF871 or BF869	6
D1,2,3,4,5,6,	9331 012 20112 BAW 62	5
D4	9331 277 60112 BZX79 C7V5	1
U1	9334 974 50112 TOA3501	1
L1, L2	(4313 020 15170) 22mH FERRITE CHOKE	2
[redacted]	[redacted]	
FERRITES	4313 020 15170 FERRITE BEAD	6
SKT1,SKT2	M3002-6A SOCKET 6 WAY	2
LINKS	'0' OHM RESISTOR	6
(UI)	M3406-28 SOCKET 28 PIN	1
WIRES	BLUE, GREEN, RED 250mmX0,65mm	3
PLUG	M3011-3A PLUG 3 WAY (3 x m2578-TL)	1
TIE	SPAG TWIST SIZE 1/8 (used above wires)	TAR

PIX BASE BOARD

R97	2123999 00011 2E2 5 Watt Standup Res	1
R95,93,94	2322 214 13152 1K5 CR68 1.15watt	3
R90	2322 211 13274 270K CR25	1
R92	2322 214 13684 680K CR68 1.15watt	1
R96	2322 212 12335 3M3 CR37	1
R91	2322 11 03364 1MEG Preset Horiz.	1
R98	2322 460 90028 Focus Pot	1
C90	2222 352 58103 10NF 400V	1
C91	2222 352 65683 68NF 630V	1
SW91,92,93	2422 136 70332 Switch	3
PL90	M2599-7A Plug 7 Way	1
PL91	M2599-3A Plug 3 Way	1
S90	3122 128 72960 Pix Base Tube Socket	1
TAG	H1918 Utilux	1
LINKS	'0' Ohm Resistor	6
PCB	820.809 Polycorp	
WIRE	60mm Grey (ex Siemens Lead)	1
FAST	Screw MT M3 x 6 Par Hd Post	1E

MAIN BOARD

R232, 235	Resistor Standup 2E2 5 Watt 2123 999 00011	2
R224	Resistor Standup 10E 5 Watt 2123 999 00012	1
R230,226	Resistor Standup 120E 5 Watt 2123 999 00013	2
R225	Resistor Standup 1K 5 Watt 2123 999 00014	1
R221	2322 212 83109 10E SR37 Safty	1
R220,222	23222 212 83278 2E7 SR37 Safty	2
R213	2322 212 13128 1E2 CR37	1
R231	2322 211 13279 27E CR25	1
R218	82E CR25	1
R219	2322 211 13829 82E CR25	1
R201	2322 211 13152 1K5 CR25	1
R211	2322 212 13222 2K2 CR 37	1
R202	2322 211 13472 4K7 CR25	1
R207,209	2322 211 13822 8K2 CR25	2
R228	2322 211 10K CR 25	1
R200	2322 211 13223 22K CR25	1
R210	2322 211 13273 27K CR25	1
R229	2322 211 13473 47K CR25	1
R234	2322 211 120K CR25	1
R204,208	2322 211 13154 150K CR25	2
R238	2322 212 13184 180K CR37 ARTWORK R232	1
R233	2322 214 13184 180K CR37	1
R223	2322 151 42204 220K MR25	1
R205	2322 211 13224 220K CR25	1
R227	2322 214 13684 680K CR68	1
R215	2322 410 03355 2K2 Preset Horiz.	1
R206,212	2322 410 03351 100E Preset Horiz.	2
R216,217	2322 410 03357 10K Preset Horiz.	2
R203	2322 410 03359 47K Preset Horiz.	1
R237	2322 594 13913 VDR	1
R236	2322 662 98009 Resistor PTC	1
C233	2212 659 00151 150PF 2KV	1
C206	2222 630 06102 1NF 100V	1
C239	2222 630 06122 1N2 100V	1
C236	2222 363 41225 2U2 250V (Non Polar)	1
C225,226, 227,228,229, 230	2212 610 11222 2N2 250VAC	6
C220	2222 357 92682 6NB 2000V	1

L200	(V25x2) Mains filter choke	2
~~L201~~	~~Degaussing Coils~~	~~2~~ PURCHASED BY POLYCORP
L202	Mains transformer	2
L203	(V15 x 2) Current sense transformer	2
L204	(V20 x 2) Base Drive Transformer	2
L205	(V25 x 2) Chopper Choke	2
L206	3122 138 35882 AT2076/70 LOPT	1
L207	Ferrite Rod 24 turns 25 SWG	1
L208	(V20 core x 2) +V20 former. Line yoke output choke. (EHT Lead - Polycorp purchase)	1
EYELETS	M2 x 2 Brass	2
EYELETS	M2 x 6 Brass	2
F. BEADS	Ferrite 4313-020-15460	4
F200	4823 253 27101 Fuse 100nA Fast	1
F202,201	4823 253 37202 Fuse 2A Slow blow	2
F203	Fuse 1.6A Fast	1
Fuse Cup	4823 492 67001 Fuse Cup	8
N200	4823 134 27602 Neon GL9	1
Focus lead	3122 131 1416 Focus lead termination	1
H/S	Heatsink for 2SD350 (SPP)	2
H/S	Heatsink for 2SD350 (DEFT)	2
H/S	Heatsink for TDA2654	1
H/S	Heatsink for L7812CV	1
PCB	820807 Polycorp	1
	Silicon Paste P4	Tar
LINKS	'0' ohm Resistor	24
WIRE	LINK TC 10mm	Tar
PL212,209,213	M2599 - 2A Plug 2 Way	3
PL205,207	M2599 - 4A Plug 4 Way	2
PL210	M2599 - 5A Plug 5 Way	1
PL2,204,1,3	M2599-6A Plug 6 Way	4
PL211	M2599 - 7A Plug 7 Way	1
PL4	M2599 - 9A Plug 9 Way	1
PL5	M2599 - 12A Plug 12 Way	1
FAST	M3 x 6 P Hd P021	3
	M3 x 8 P Hd P021	2
	M3 x 16 P Hd P021	4
	NUT M3 HEX Machine	15
	WASHER M3 INT	15
	WASHER 1/8 x 3/8 Flat	10
	TO3 M/HARDWARE SETS	2
	TO3 MICA WASHER	2

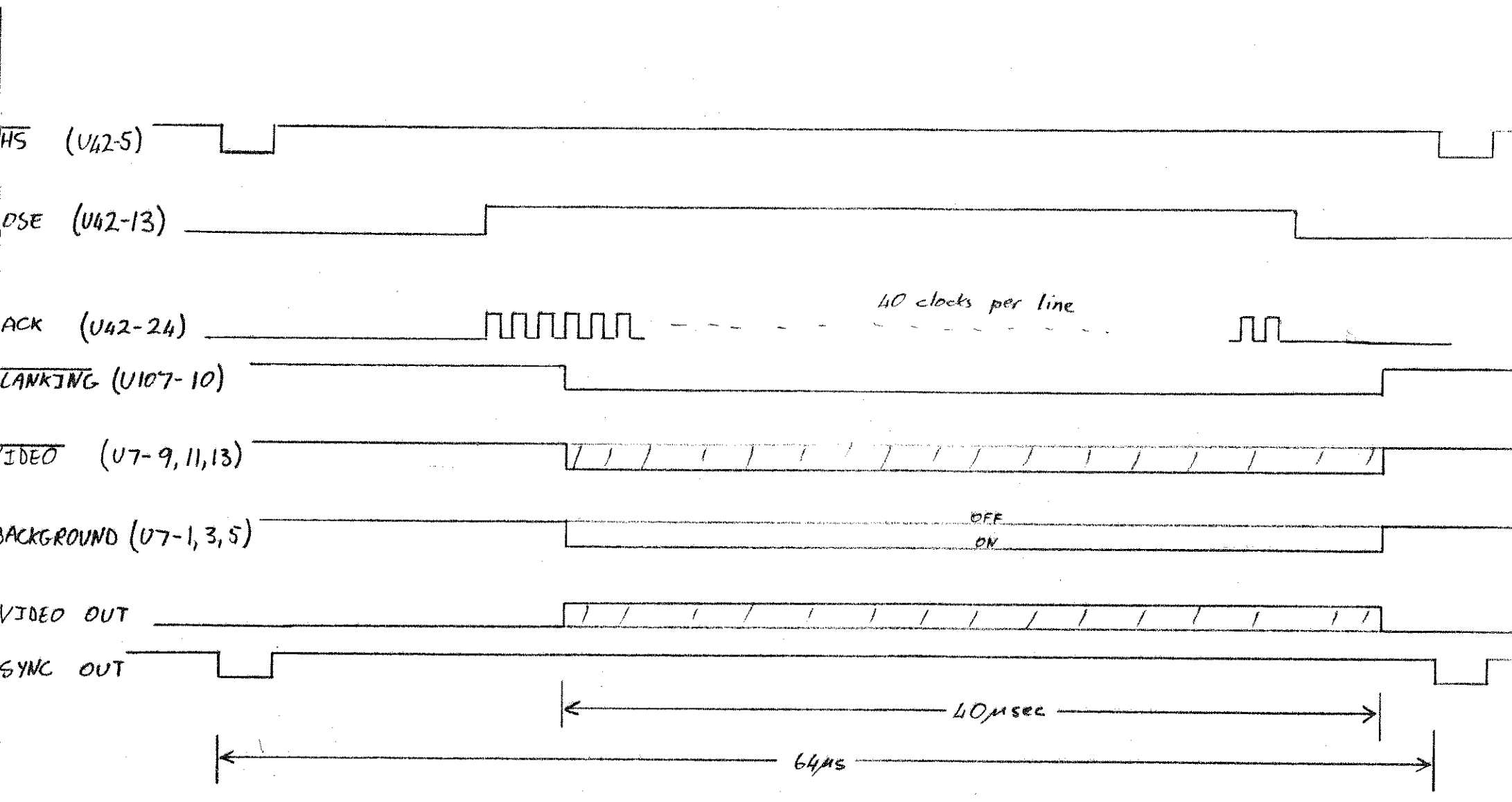
C232	2222	084	58221	220uF 375V	1
C216	2222	001	66471	470uF 25V	1
C211,237	2222	034	67471	470uF 40V	2
D218,201, 202,203,204	9333	929	30113	BAX18A	5
D209	9331	892	10112	BAV21 (BAV19)	1
D217	9331	012	20112	BAW62	1
D200	9334	752	20112	BY 257 Bridge	1
D216	9331	206	60112	BY184	1
D215	9332	024	20113	BY1888	1
D206,210	9334	452	80112	BY228	2
D205,213,214	9335	001	70113	BYV95B Subs t BY406	3
D211,212	9335	001	70113	BYV958	2
D207,208	9335	001	80112	BYV95C	2
T200,201	9332	762	20112	2SD350A	2
U200	9334	843	30112	TDA2654	1
U201	9323	999	50021	L7812CV Regulator	1
C200				10NF 63V	1
C235	2222	357	90078	10N5 2000V	1
C218	2222	341	80103	10NF 1600V	1
C234	2222	352	48473	47NF 250V	1
C240,241	2222	330	40104	100NF 250VAC	2
C201	2222	352	48154	150NF 250V	1
C219	2222	357	52334	330NF 250V	1
C224	2222	330	40334	330NF 250VAC	!
C238	2222	352	28224	220NF 100V	1
C231	2222	352	58474	470NF 400V	1
C202,207 212,222	2222	352	47104	100NF 250V	4
C221	2222	352	28684	680NF 100V	1
C213	2222	034	58228	2u2 63V	1
C217	2222	031	65228	2U2 250V	1
C209	2222	034	57478	4U7 40V	1
C210	2222	034	58109	10uF 63V	1
C204	2222	034	57229	22uF 40V	1
C223	2222	034	54479	47uF 10V	1
C203,205	2222	034	66101	100uF 25V	2
C208,215	2222	034	68101	100uF 63V	2
C214	2222	042	11101	100uF 160V	1

C A B L E S

Video to Computer Cable	Length 450mm	
5 way keyed 1-2 housing	M3011-5A	1
6 way no key housing	M3001-6A	1
TERMINALS	M2578-GL	10
Lengths of ELV Hook up Wire- 450mm long	0.5mm² Stranded	5

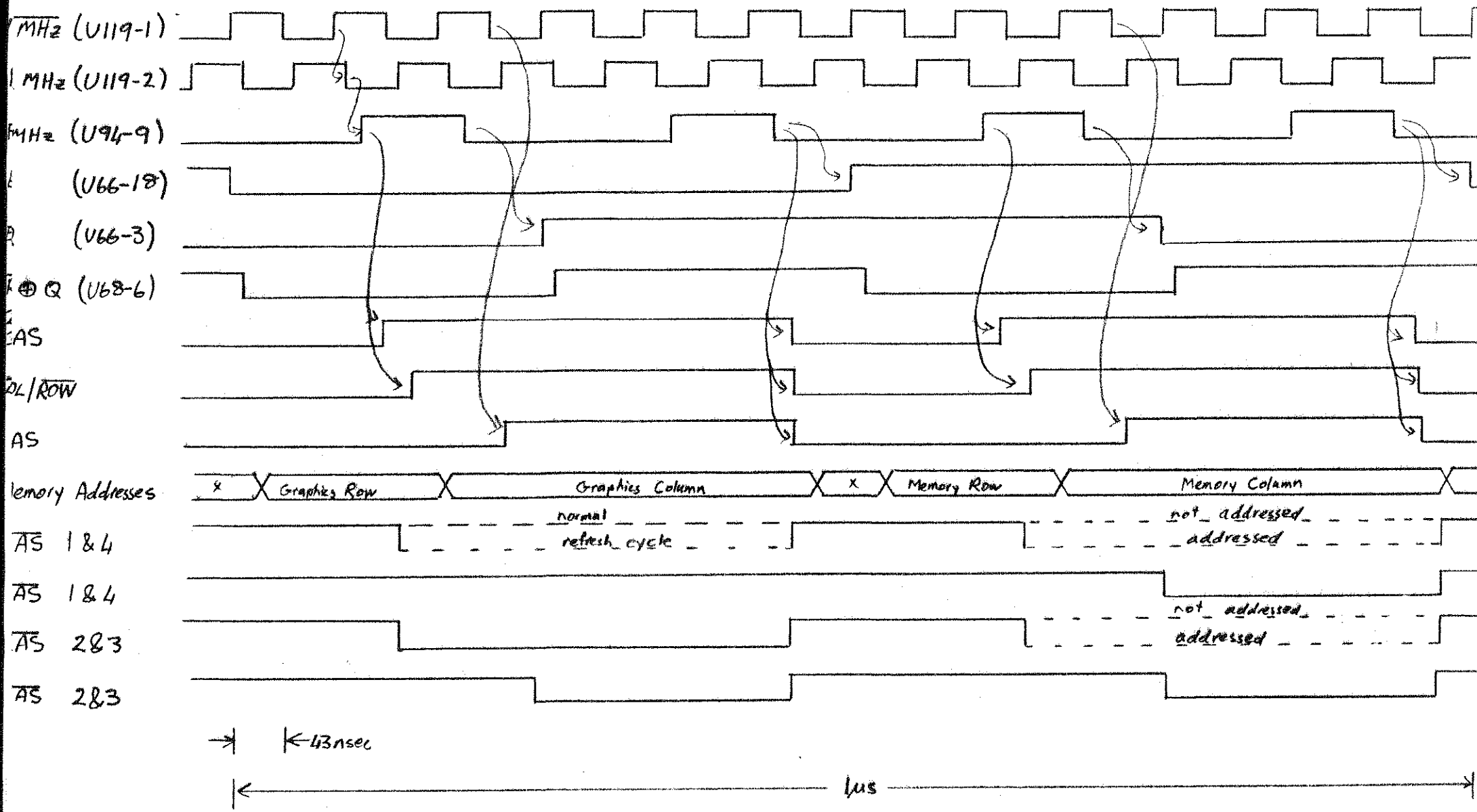
PICTURE TUBE BASE LEAD

7 way no key	M 3001-7A	2
TERMINALS	M 2578-GL	14
Lengths of ELV Hook-up Wire 500mm long	0.5mm² Stranded	7

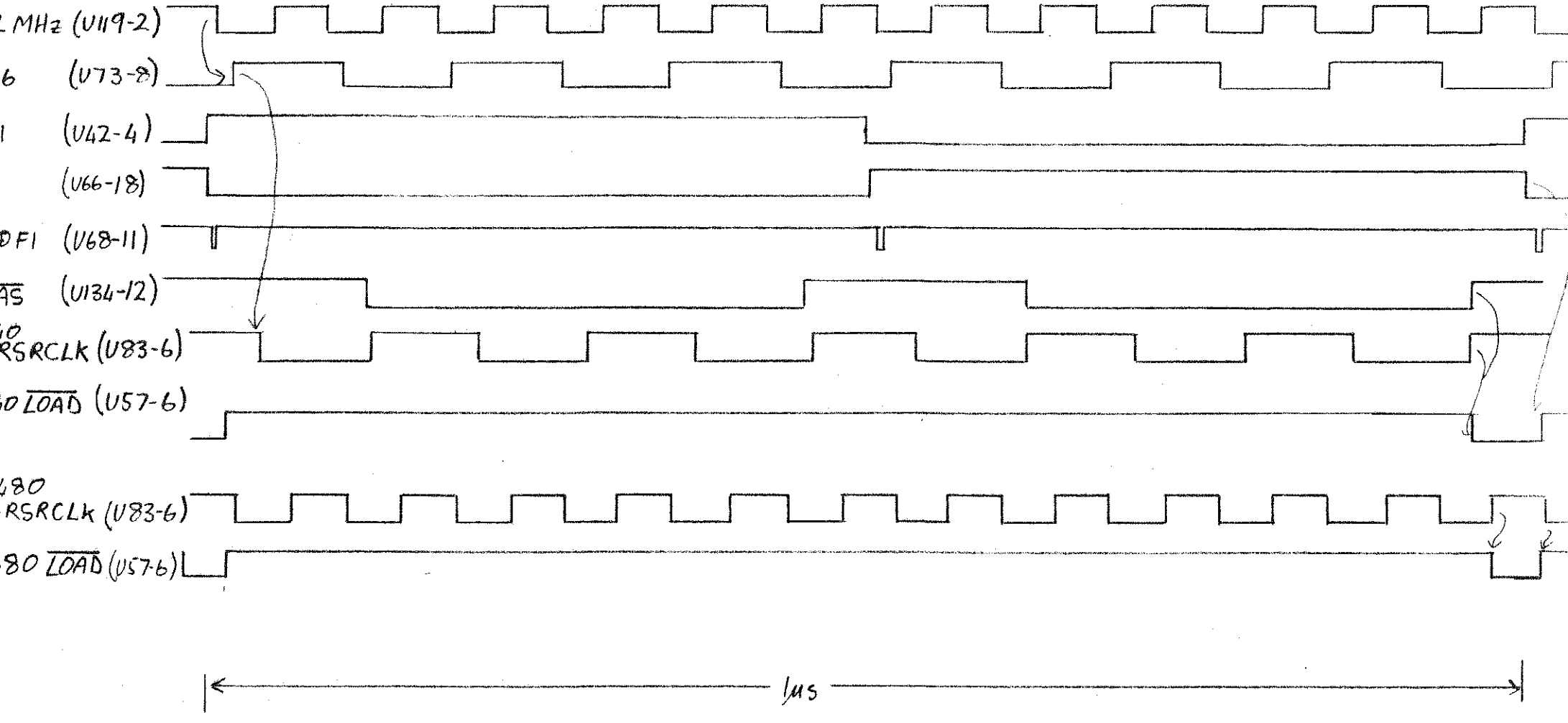


Video Out 0.7v p-p into 75 ohms. Sync Out 2v p-p into 75 ohms

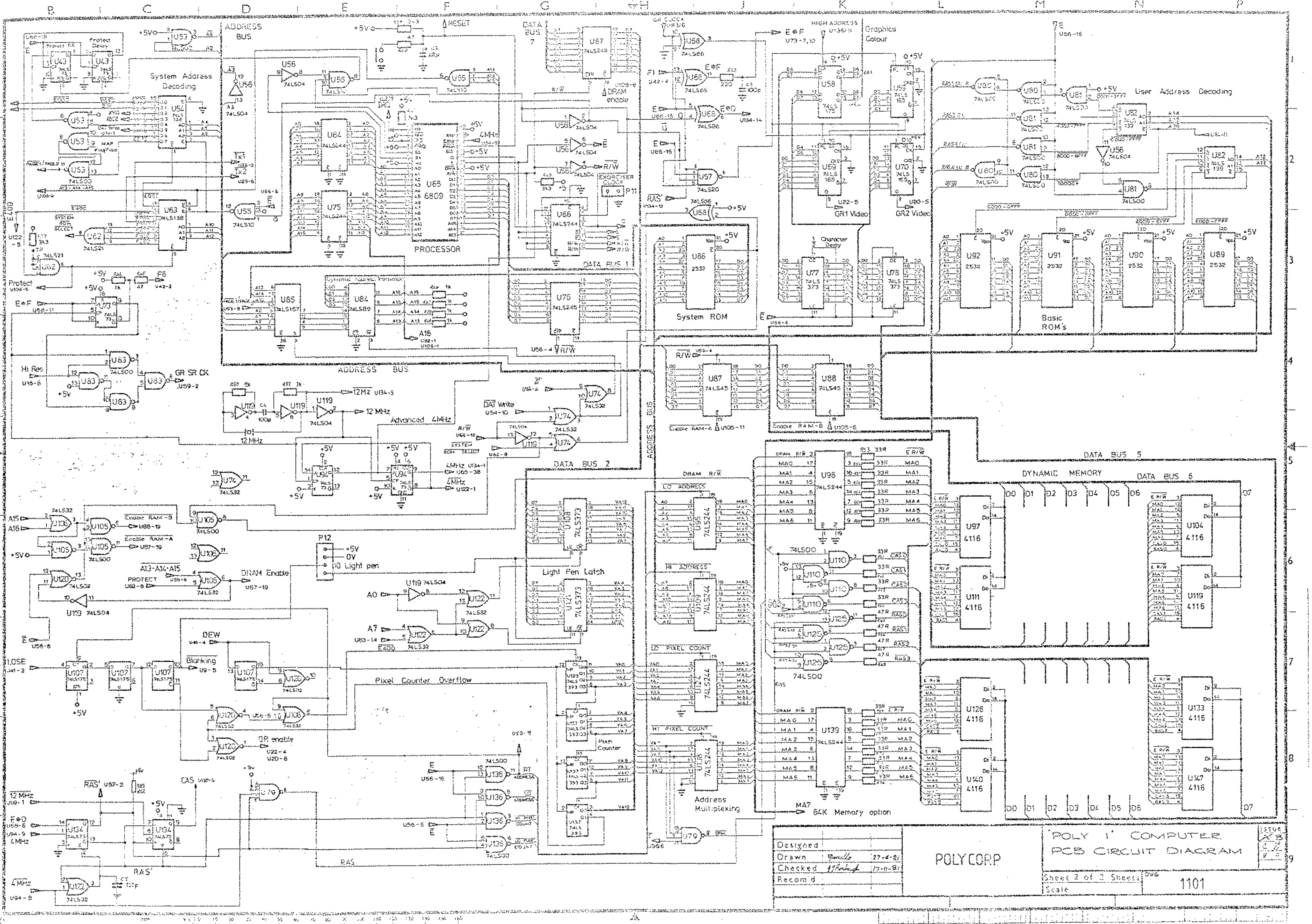
POLY-1 VIDEO TIMING

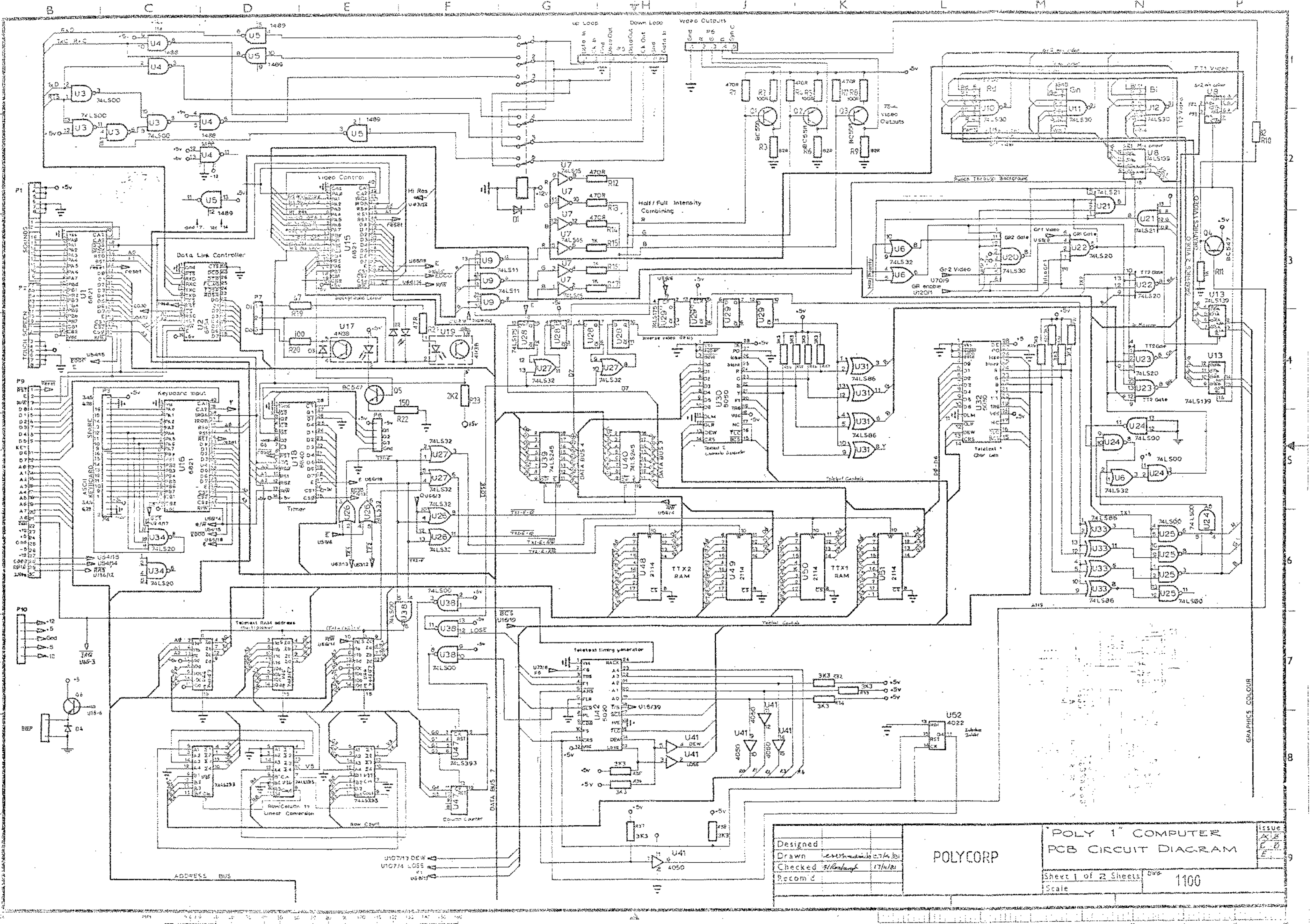


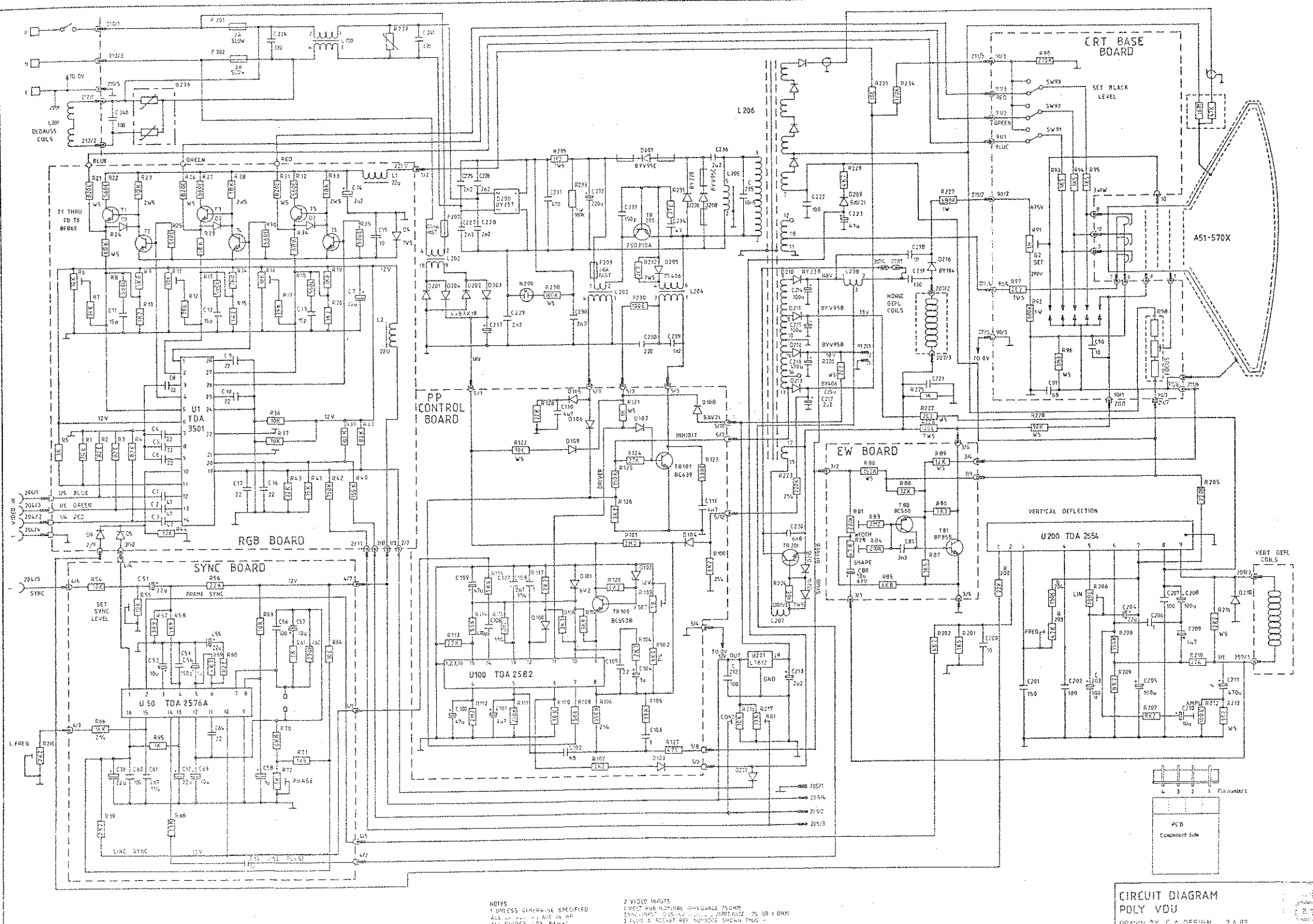
POLY-1 DYNAMIC MEMORY TIMING



POLY-1 GRAPHICS TIMING

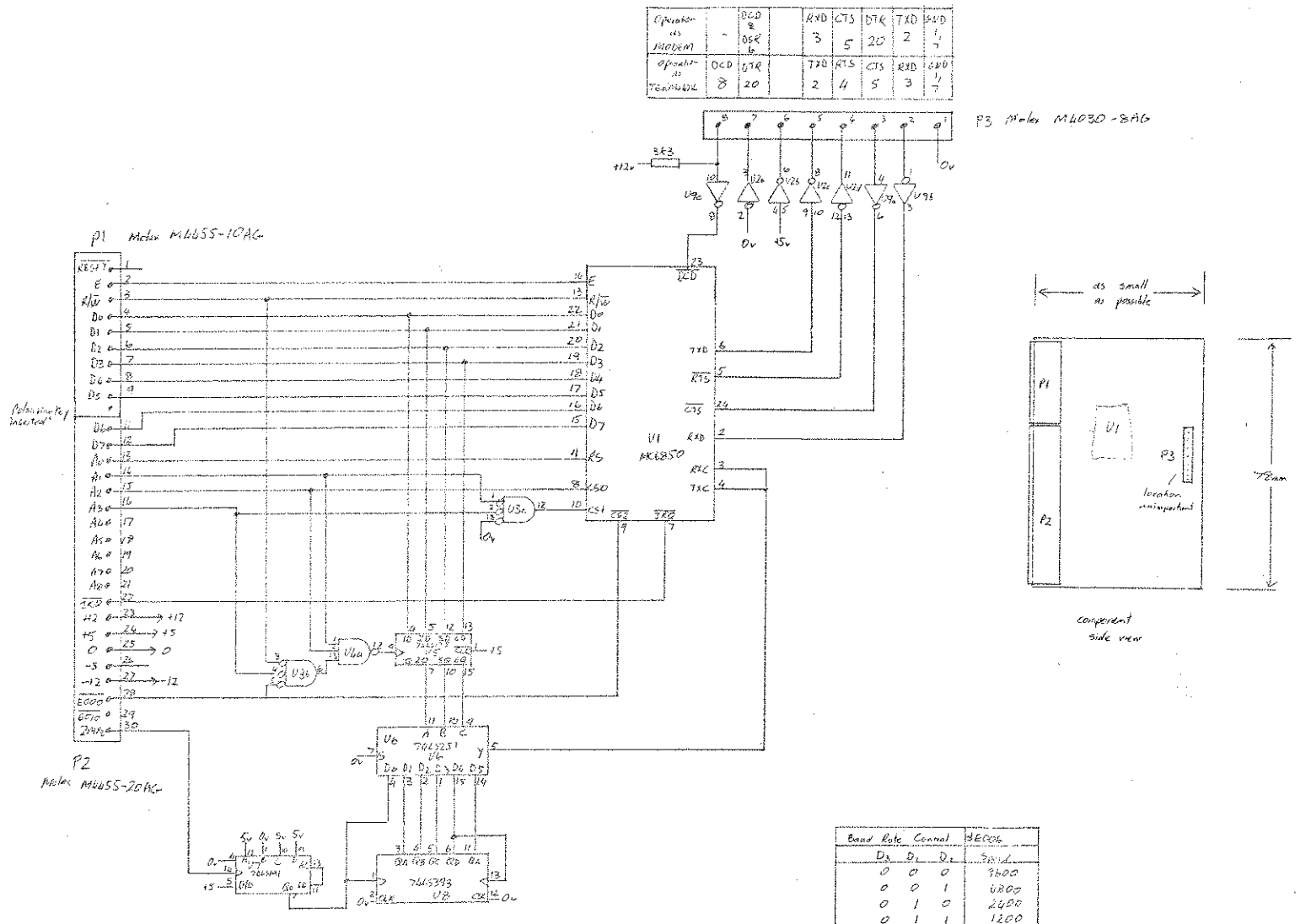

System Address Decoding
ADDRESS BUS
PROCESSOR
U65 6809
DATA BUS 1
DATA BUS 2
DATA BUS 5
DATA BUS 6
DATA BUS 7
System ROM
Basic ROM's
User Address Decoding
GR1 Video
GR2 Video
Graphics Colour
HIGH ADDRESS
Character Delay
Light Pen Latch
Pixel Counter Overflow
Pixel Counter
Address Multiplexing
DYNAMIC MEMORY
64K Memory option
LO ADDRESS
HI ADDRESS
LO PIXEL COUNT
HI PIXEL COUNT
DRAM R/W
DRAM Enable
Enable RAM-A
Enable RAM-B
Advanced 4MHz
12 MHz
Light pen
Blanking
GR enable
GR SR CK
Hi Res
Protect
RESET
EXORCISER CLOCK
DEW
Designed
Drawn
Checked
Recom'd
27-4-81
17-11-81
POLYCORP
"POLY 1" COMPUTER
PCB CIRCUIT DIAGRAM
Sheet 2 of 2 Sheets
Scale
DWG 1101


"POLY 1" COMPUTER
PCB CIRCUIT DIAGRAM
POLYCORP
Designed
Drawn
Checked
Recom'd
Sheet 1 of 2 Sheets
Scale
1100
Issue



NOTES
1 UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE IN Ω
ALL CAPACITORS ARE IN μF
2 VIDEO INPUTS
1 VOLT PEAK NOMINAL (ADJUSTABLE 75 OHM
SYNC INPUT 0.15-5V (HIGH IMPEDANCE 75 OR 1 OHM
3 PLUG & SOCKET PIN NUMBERS SHOWN THUS —

CIRCUIT DIAGRAM
POLY VOU
DRAWN BY C.A. DESIGN 2.6.87



POLYCORP

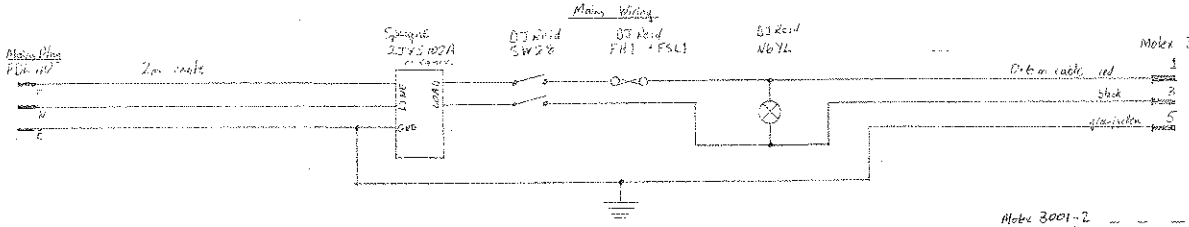
POLY-1

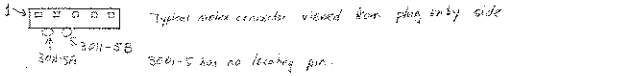
RS 232 Interface.

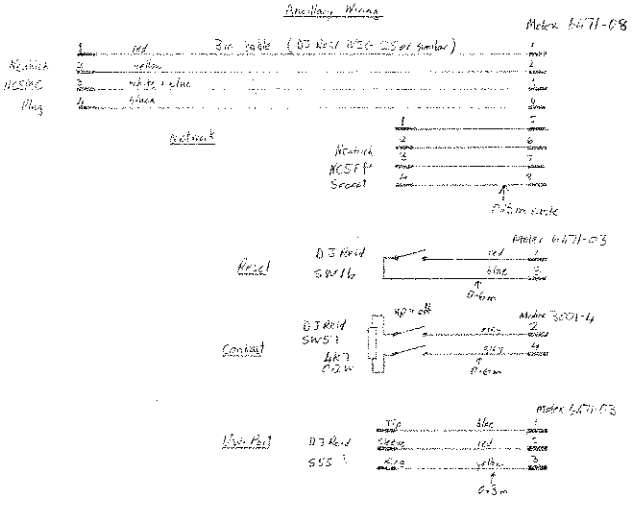
SHEET

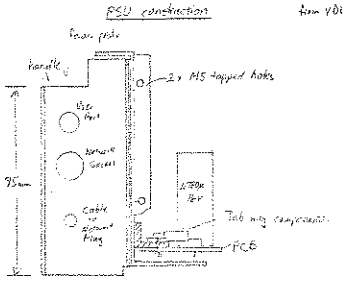
DRAWN | CHECKED | SCALE | SERIES OF

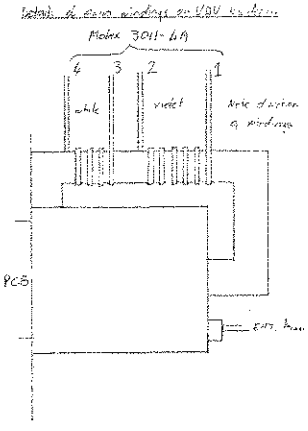
TRACED | DATE | REF

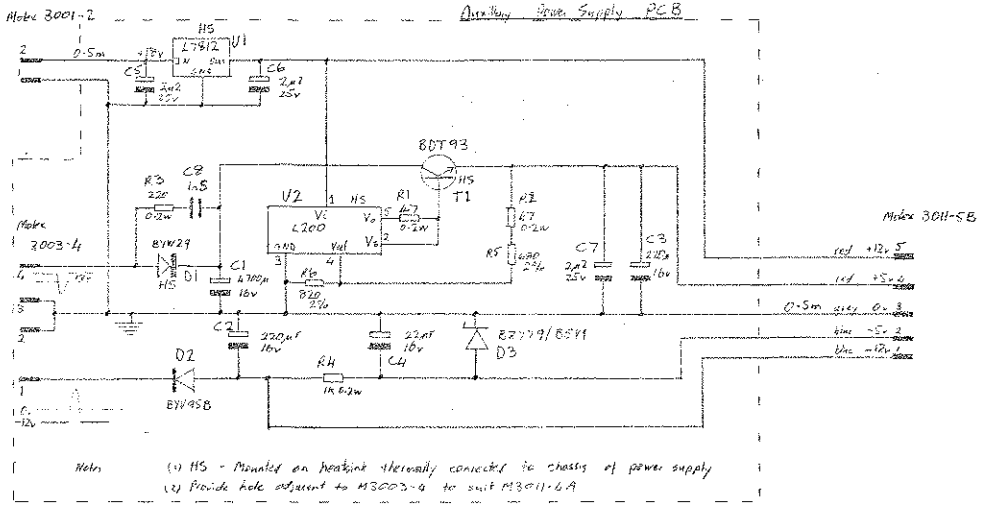












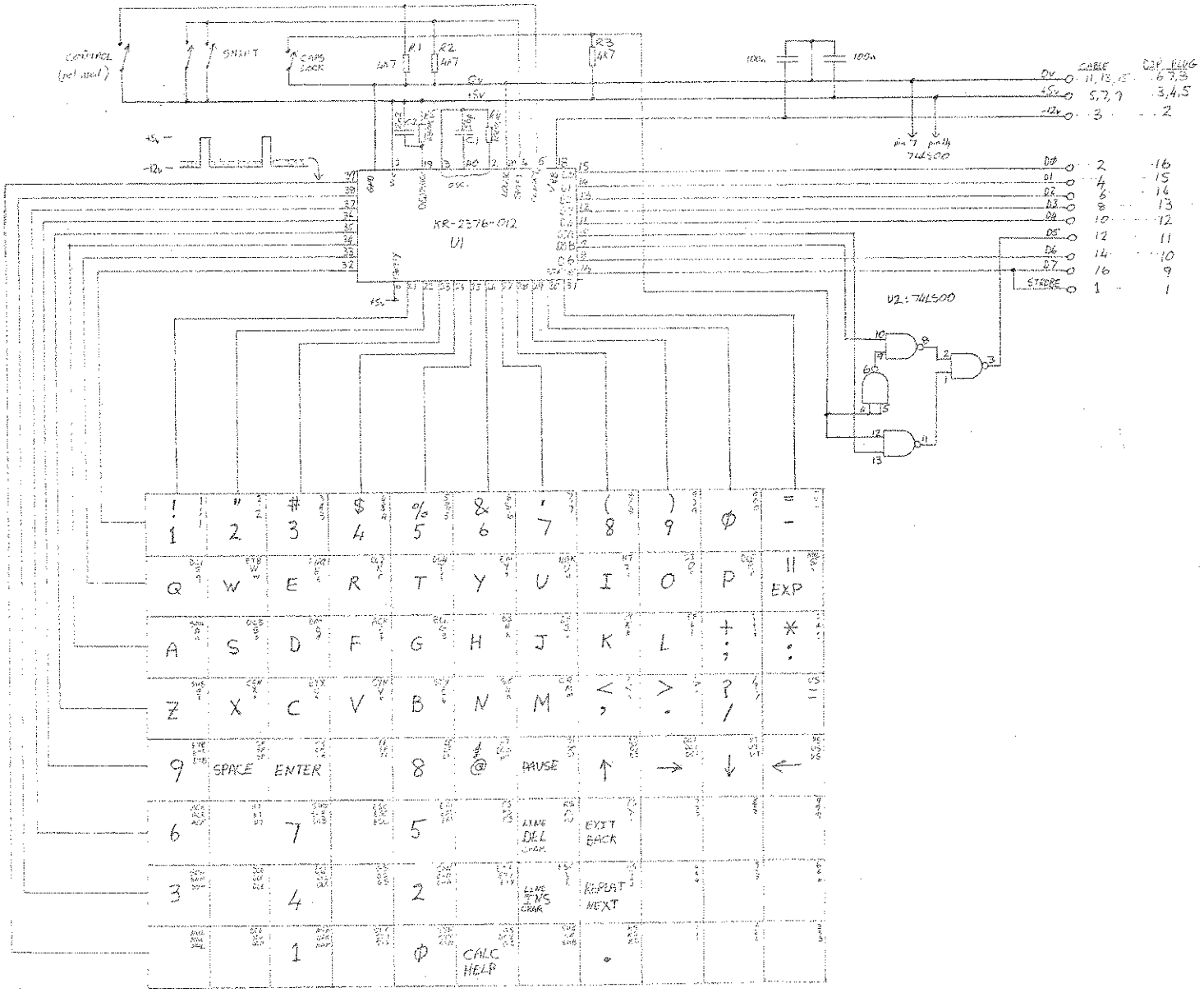
Ancillary Power Supply Parts List

			Philips Code		
1 ×	BYW29	Fast diode	9333	912	80112
1 ×	BYW95B	Fast diode	9335	001	70113
1 ×	BZY79/B5V1	Zener	9331	668	10112
1 ×	L200CV	Regulator	9323	999	50057
1 ×	L7812	Regulator	9323	999	50021
1 ×	BDT93	Transistor	9334	519	10112
1 ×	4·7Ω	CR25	2322	211	13478
1 ×	1k	CR25	2322	211	13102
1 ×	47Ω	CR25	2322	211	13479
1 ×	220Ω	CR25	2322	211	13221
1 ×	680	MR25	2322	151	56801
1 ×	820	MR25	2322	151	58201
1 ×	4700µF 16V	High Ripple	2222	050	55472
2 ×	220µF 16V	Electro	2222	034	65221
1 ×	22µF 16V	Electro	2222	034	65229
3 ×	2µ2 25V	Solid Al.	2222	122	56229
1 ×	1nS	Cer. plate	2222	630	06152

POLYCORP

POLY-1 POWER SUPPLY MK2

DRAWN T. Eastwood
CHECKED
DATE 13-4-82
SCALES
DWG 1401
SERIES OF
REF



POLYCORP

ZX-1 KEYBOARD
Circuit Diagram

DRAWN
TRACED
CHECKED
DATE 16/4/81
SCALES

DWG
1500

SERIES OF
ISS